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**M393B2G70AH0**
**M393B2G73AH0**
**M393B4G70AM0**

# 240pin Registered DIMM based on 4Gb A-die

## 78FBGA with Lead-Free & Halogen-Free (RoHS compliant)

datasheet

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# 1. DDR3 Registered DIMM Ordering Information

| Part Number[2] | Density | Organization | Component Composition | Number of Rank | Height |
|---|---|---|---|---|---|
| M393B2G70AH0-CF8/H9 | 16GB | 2Gx72 | 1Gx4(K4B4G0446A-HC##)*36 | 2 | 30mm |
| M393B2G73AH0-CF8/H9 | 16GB | 2Gx72 | 512Mx8(K4B4G0846A-HC##)*36 | 4 | 30mm |
| M393B4G70AM0-CF8/H9 | 32GB | 4Gx72 | DDP 2Gx4(K4B8G0446A-MC##)*36 | 4 | 30mm |

**NOTE** :
1. "##" - F8/H9
2. F8(1066Mbps 7-7-7) / H9(1333Mbps 9-9-9)
   - DDR3-1333(9-9-9) is backward compatible to DDR3-1066(7-7-7)

# 2. Key Features

| Speed | DDR3-800 | DDR3-1066 | DDR3-1333 | Unit |
|---|---|---|---|---|
| | 6-6-6 | 7-7-7 | 9-9-9 | |
| tCK(min) | 2.5 | 1.875 | 1.5 | ns |
| CAS Latency | 6 | 7 | 9 | nCK |
| tRCD(min) | 15 | 13.125 | 13.5 | ns |
| tRP(min) | 15 | 13.125 | 13.5 | ns |
| tRAS(min) | 37.5 | 37.5 | 36 | ns |
| tRC(min) | 52.5 | 50.625 | 49.5 | ns |

- JEDEC standard 1.5V ± 0.075V Power Supply
- $V_{DDQ}$ = 1.5V ± 0.075V
- 400MHz $f_{CK}$ for 800Mb/sec/pin, 533MHz $f_{CK}$ for 1066Mb/sec/pin, 667MHz $f_{CK}$ for 1333Mb/sec/pin
- 8 independent internal bank
- Programmable $\overline{CAS}$ Latency: 6,7,8,9
- Programmable Additive Latency(Posted $\overline{CAS}$) : 0, CL - 2, or CL - 1 clock
- Programmable $\overline{CAS}$ Write Latency(CWL) = 5(DDR3-800), 6(DDR3-1066) and 7(DDR3-1333)
- Burst Length: 8 (Interleave without any limit, sequential with starting address “000” only), 4 with tCCD = 4 which does not allow seamless read or write [either On the fly using A12 or MRS]
- Bi-directional Differential Data Strobe
- On Die Termination using ODT pin
- Average Refresh Period 7.8us at lower then $T_{CASE}$ 85°C, 3.9us at 85°C < $T_{CASE} \leq$ 95°C
- Asynchronous Reset

# 3. Address Configuration

| Organization | Row Address | Column Address | Bank Address | Auto Precharge |
|---|---|---|---|---|
| 1Gx4(4Gb) based Module | A0-A15 | A0-A9, A11 | BA0-BA2 | A10/AP |
| 512Mx8(4Gb) based Module | A0-A15 | A0-A9 | BA0-BA2 | A10/AP |
| 2Gx4(8Gb DDP) based Module | A0-A15 | A0-A9, A11 | BA0-BA2 | A10/AP |

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# 4. Registered DIMM Pin Configurations (Front side/Back side)

| Pin | Front | Pin | Back | Pin | Front | Pin | Back | Pin | Front | Pin | Back |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $V_{REFDQ}$ | 121 | $V_{SS}$ | 42 | $\overline{DQS8}$ | 162 | NC,$\overline{DQS17}$ ,$\overline{TDQS17}$ | 82 | DQ33 | 202 | $V_{SS}$ |
| 2 | $V_{SS}$ | 122 | DQ4 | 43 | DQS8 | 163 | $V_{SS}$ | 83 | $V_{SS}$ | 203 | DM4,DQS13 ,$\overline{TDQS13}$ |
| 3 | DQ0 | 123 | DQ5 | 44 | $V_{SS}$ | 164 | CB6,NC | 84 | $\overline{DQS4}$ | 204 | NC,$\overline{DQS13}$ ,$\overline{TDQS13}$ |
| 4 | DQ1 | 124 | $V_{SS}$ | 45 | CB2,NC | 165 | CB7,NC | 85 | DQS4 | 205 | $V_{SS}$ |
| 5 | $V_{SS}$ | 125 | DM0,DQS9 ,$\overline{TDQS9}$ | 46 | CB3,NC | 166 | $V_{SS}$ | 86 | $V_{SS}$ | 206 | DQ38 |
| 6 | $\overline{DQS0}$ | 126 | NC,$\overline{DQS9}$ ,$\overline{TDQS9}$ | 47 | $V_{SS}$ | 167 | NC(TEST) | 87 | DQ34 | 207 | DQ39 |
| 7 | DQS0 | 127 | $V_{SS}$ | 48 | $V_{TT}$, NC | 168 | $\overline{RESET}$ | 88 | DQ35 | 208 | $V_{SS}$ |
| 8 | $V_{SS}$ | 128 | DQ6 | KEY | | | | 89 | $V_{SS}$ | 209 | DQ44 |
| 9 | DQ2 | 129 | DQ7 | 49 | $V_{TT}$, NC | 169 | CKE1, NC | 90 | DQ40 | 210 | DQ45 |
| 10 | DQ3 | 130 | $V_{SS}$ | 50 | CKE0 | 170 | $V_{DD}$ | 91 | DQ41 | 211 | $V_{SS}$ |
| 11 | $V_{SS}$ | 131 | DQ12 | 51 | $V_{DD}$ | 171 | A15 | 92 | $V_{SS}$ | 212 | DM5,DQS14 ,$\overline{TDQS14}$ |
| 12 | DQ8 | 132 | DQ13 | 52 | BA2 | 172 | A14 | 93 | $\overline{DQS5}$ | 213 | NC,$\overline{DQS14}$ ,$\overline{TDQS14}$ |
| 13 | DQ9 | 133 | $V_{SS}$ | 53 | $\overline{Err\_Out}$/NC | 173 | $V_{DD}$ | 94 | DQS5 | 214 | $V_{SS}$ |
| 14 | $V_{SS}$ | 134 | DM1,DQS10 ,$\overline{TDQS10}$ | 54 | $V_{DD}$ | 174 | A12/$\overline{BC}$ | 95 | $V_{SS}$ | 215 | DQ46 |
| 15 | $\overline{DQS1}$ | 135 | NC,$\overline{DQS10}$ ,$\overline{TDQS10}$ | 55 | A11 | 175 | A9 | 96 | DQ42 | 216 | DQ47 |
| 16 | DQS1 | 136 | $V_{SS}$ | 56 | A7 | 176 | $V_{DD}$ | 97 | DQ43 | 217 | $V_{SS}$ |
| 17 | $V_{SS}$ | 137 | DQ14 | 57 | $V_{DD}$ | 177 | A8 | 98 | $V_{SS}$ | 218 | DQ52 |
| 18 | DQ10 | 138 | DQ15 | 58 | A5 | 178 | A6 | 99 | DQ48 | 219 | DQ53 |
| 19 | DQ11 | 139 | $V_{SS}$ | 59 | A4 | 179 | $V_{DD}$ | 100 | DQ49 | 220 | $V_{SS}$ |
| 20 | $V_{SS}$ | 140 | DQ20 | 60 | $V_{DD}$ | 180 | A3 | 101 | $V_{SS}$ | 221 | DM6,DQS15 ,$\overline{TDQS15}$ |
| 21 | DQ16 | 141 | DQ21 | 61 | A2 | 181 | A1 | 102 | $\overline{DQS6}$ | 222 | NC,$\overline{DQS15}$ ,$\overline{TDQS15}$ |
| 22 | DQ17 | 142 | $V_{SS}$ | 62 | $V_{DD}$ | 182 | $V_{DD}$ | 103 | DQS6 | 223 | $V_{SS}$ |
| 23 | $V_{SS}$ | 143 | DM2,DQS11 ,$\overline{TDQS11}$ | 63 | NC, CK1 | 183 | $V_{DD}$ | 104 | $V_{SS}$ | 224 | DQ54 |
| 24 | $\overline{DQS2}$ | 144 | NC,$\overline{DQS11}$ ,$\overline{TDQS11}$ | 64 | NC, $\overline{CK1}$ | 184 | CK0 | 105 | DQ50 | 225 | DQ55 |
| 25 | DQS2 | 145 | $V_{SS}$ | 65 | $V_{DD}$ | 185 | $\overline{CK0}$ | 106 | DQ51 | 226 | $V_{SS}$ |
| 26 | $V_{SS}$ | 146 | DQ22 | 66 | $V_{DD}$ | 186 | $V_{DD}$ | 107 | $V_{SS}$ | 227 | DQ60 |
| 27 | DQ18 | 147 | DQ23 | 67 | $V_{REFCA}$ | 187 | $\overline{EVENT}$,NC | 108 | DQ56 | 228 | DQ61 |
| 28 | DQ19 | 148 | $V_{SS}$ | 68 | NC/Par_In | 188 | A0 | 109 | DQ57 | 229 | $V_{SS}$ |
| 29 | $V_{SS}$ | 149 | DQ28 | 69 | $V_{DD}$ | 189 | $V_{DD}$ | 110 | $V_{SS}$ | 230 | DM7/DQS16 $\overline{TDQS16}$ |
| 30 | DQ24 | 150 | DQ29 | 70 | A10/AP | 190 | BA1 | 111 | $\overline{DQS7}$ | 231 | DM7,DQS16 ,$\overline{TDQS16}$ |
| 31 | DQ25 | 151 | $V_{SS}$ | 71 | BA0 | 191 | $V_{DD}$ | 112 | DQS7 | 232 | $V_{SS}$ |
| 32 | $V_{SS}$ | 152 | DM3,DQS12 ,$\overline{TDQS12}$ | 72 | $V_{DD}$ | 192 | $\overline{RAS}$ | 113 | $V_{SS}$ | 233 | DQ62 |
| 33 | $\overline{DQS3}$ | 153 | NC,$\overline{DQS12}$ ,$\overline{TDQS12}$ | 73 | $\overline{WE}$ | 193 | $\overline{S0}$ | 114 | DQ58 | 234 | DQ63 |
| 34 | DQS3 | 154 | $V_{SS}$ | 74 | $\overline{CAS}$ | 194 | $V_{DD}$ | 115 | DQ59 | 235 | $V_{SS}$ |
| 35 | $V_{SS}$ | 155 | DQ30 | 75 | $V_{DD}$ | 195 | ODT0 | 116 | $V_{SS}$ | 236 | $V_{DDSPD}$ |
| 36 | DQ26 | 156 | DQ31 | 76 | $\overline{S1}$,NC | 196 | A13 | 117 | SA0 | 237 | SA1 |
| 37 | DQ27 | 157 | $V_{SS}$ | 77 | ODT1,NC | 197 | $V_{DD}$ | 118 | SCL | 238 | SDA |
| 38 | $V_{SS}$ | 158 | CB4,NC | 78 | $V_{DD}$ | 198 | $\overline{S3}$,NC | 119 | SA2 | 239 | $V_{SS}$ |
| 39 | CB0,NC | 159 | CB5,NC | 79 | $\overline{S2}$,NC | 199 | $V_{SS}$ | 120 | $V_{TT}$ | 240 | $V_{TT}$ |
| 40 | CB1,NC | 160 | $V_{SS}$ | 80 | $V_{SS}$ | 200 | DQ36 | | | | |
| 41 | $V_{SS}$ | 161 | DM8,DQS17 TDQS17,NC | 81 | DQ32 | 201 | DQ37 | | | | |

**NOTE** : NC = No internal Connection

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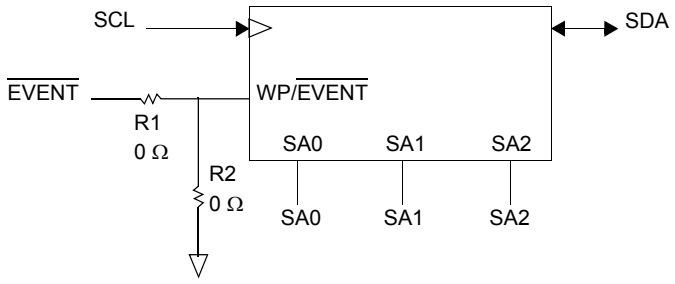
# 5. Pin Description

| Pin Name | Description | Number | Pin Name | Description | Number |
|---|---|---|---|---|---|
| CK0 | Clock Input, positive line | 1 | ODT[1:0] | On Die Termination Inputs | 2 |
| $\overline{CK0}$ | Clock Input, negative line | 1 | DQ[63:0] | Data Input/Output | 64 |
| CKE[1:0] | Clock Enables | 2 | CB[7:0] | Data check bits Input/Output | 8 |
| $\overline{RAS}$ | Row Address Strobe | 1 | DQS[8:0] | Data strobes | 9 |
| $\overline{CAS}$ | Column Address Strobe | 1 | $\overline{DQS}$[8:0] | Data strobes, negative line | 9 |
| $\overline{WE}$ | Write Enable | 1 | DM[8:0]/ DQS[17:9] TDQS[17:9] | Data Masks/ Data strobes, Termination data strobes | 9 |
| $\overline{S}$[3:0] | Chip Selects | 4 | $\overline{DQS}$[17:9] $\overline{TDQS}$[17:9] | Data strobes, negative line, Termination data strobes | 9 |
| A[9:0],A11, A[15:13] | Address Inputs | 2\14 | RFU | Reserved for Future Use | 2 |
| A10/AP | Address Input/Autoprecharge | 1 | $\overline{EVENT}$ | Reserved for optional hardware temperature sensing | 1 |
| A12/$\overline{BC}$ | Address Input/Burst chop | 1 | TEST | Memory bus test toll (Not Connected and Not Usable on DIMMs) | 1 |
| BA[2:0] | SDRAM Bank Addresses | 3 | $\overline{RESET}$ | Register and SDRAM control pin | 1 |
| SCL | Serial Presence Detect (SPD) Clock Input | 1 | $V_{DD}$ | Power Supply | 22 |
| SDA | SPD Data Input/Output | 1 | $V_{SS}$ | Ground | 59 |
| SA[2:0] | SPD Address Inputs | 3 | $V_{REFDQ}$ | Reference Voltage for DQ | 1 |
| Par_In | Parity bit for the Address and Control bus | 1 | $V_{REFCA}$ | Reference Voltage for CA | 1 |
| $\overline{Err\_Out}$ | Parity error found on the Address and Control bus | 1 | $V_{TT}$ | Termination Voltage | 4 |
| | | | $V_{DDSPD}$ | SPD Power | 1 |
| | | | | Total | 240 |

**NOTE** :
*The $V_{DD}$ and $V_{DDQ}$ pins are tied common to a single power-plane on these designs.

# 6. ON DIMM Thermal Sensor




**NOTE** : 1. All Samsung RDIMM support Thermal sensor on DIMM
2. When the SPD and the thermal sensor are placed on the module, R1 is placed but R2 is not.
When only the SPD is placed on the module, R2 is placed but R1 is not.

**[ Table 1 ] Temperature Sensor Characteristics**

| Grade | Range | Temperature Sensor Accuracy | | | Units | NOTE |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| B | 75 < Ta < 95 | - | +/- 0.5 | +/- 1.0 | °C | - |
| | 40 < Ta < 125 | - | +/- 1.0 | +/- 2.0 | | - |
| | -20 < Ta < 125 | - | +/- 2.0 | +/- 3.0 | | - |
| Resolution | | 0.25 | | | °C /LSB | - |

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# 7. Input/Output Functional Description

| Symbol | Type | Polarity | Function |
|---|---|---|---|
| CK0 | Input | Positive Edge | Positive line of the differential pair of system clock inputs that drives input to the on-DIMM Clock Driver. |
| $\overline{CK0}$ | Input | Negative Edge | Negative line of the differential pair of system clock inputs that drives the input to the on-DIMM Clock Driver. |
| CKE[1:0] | Input | Active High | CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers of the SDRAMs. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWER DOWN (row ACTIVE in any bank) |
| $\overline{S}$[3:0] | Input | Active Low | Enables the associated SDRAM command decoder when low and disables decoder when high. When decoder is disabled, new commands are ignored and previous operations continue. These input signals also disable all outputs (except CKE and ODT) of the register(s) on the DIMM when both inputs are high. When both S[1:0] are high, all register outputs (except CKE, ODT and Chip select) remain in the previous state. For modules supporting 4 ranks, S[3:2] operate similarly to S[1:0] for a second set of register outputs. |
| ODT[1:0] | Input | Active High | On-Die Termination control signals |
| $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | Input | Active Low | When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM. |
| $V_{REFDQ}$ | Supply | | Reference voltage for DQ0-DQ63 and CB0-CB7 |
| $V_{REFCA}$ | Supply | | Reference voltage for A0-A15, BA0-BA2, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{S0}$, $\overline{S1}$, CKE0, CKE1, Par_In, ODT0 and ODT1. |
| BA[2:0] | Input | | Selects which SDRAM bank of eight is activated. BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines mode register is to be accessed during an MRS cycle. |
| A[15:13, 12/BC,11, 10/AP,9:0] | Input | | Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA. A12 is also utilized for BL 4/8 identification for "BL on the fly" during CAS command. The address inputs also provide the op-code during Mode Register Set commands. |
| DQ[63:0], CB[7:0] | I/O | | Data and Check Bit Input/Output pins |
| DM[8:0] | | | Active High Masks write data when high, issued concurrently with input data. $V_{DD}$, $V_{SS}$ Supply Power and ground for the DDR SDRAM input buffers and core logic. $V_{TT}$ Supply Termination Voltage for Address/Command/Control/Clock nets. |
| DQS[17:0] | I/O | | Positive Edge Positive line of the differential data strobe for input and output data. |
| $\overline{DQS}$[17:0] | I/O | | Negative Edge Negative line of the differential data strobe for input and output data. |
| TDQS[17:9], $\overline{TDQS}$[17:9] | OUT | | TDQS/$\overline{TDQS}$ is applicable for X8 DRAMs only. When enabled via Mode Register A11=1 in MR1, DRAM will enable the same termination resistance function on TDQS/$\overline{TDQS}$ that is applied to DQS/$\overline{DQS}$. When disabled via mode register A11=0 in MR1, DM/TDQS will provide the data mask function and TDQS is not used. X4/X16 DRAMs must disable the TDQS function via mode register A11=0 in MR1 |
| SA[2:0] | IN | | These signals are tied at the system planar to either $V_{SS}$ or $V_{DDSPD}$ to configure the serial SPD EEPROM address range. |
| SDA | I/O | | This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to $V_{DDSPD}$ on the system planar to act as a pull-up. |
| SCL | IN | | This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to $V_{DDSPD}$ on the system planar to act as a pull-up. |
| $\overline{EVENT}$ | OUT (open drain) | Active Low | This signal indicates that a thermal event has been detected in the thermal sensing device.The system should guarantee the electrical level requirement is met for the $\overline{EVENT}$ pin on TS/SPD part. |
| $V_{DDSPD}$ | Supply | | Serial EEPROM positive power supply wired to a separate power pin at the connector which supports from 3.0 Volt to 3.6 Volt (nominal 3.3V) operation. |
| $\overline{RESET}$ | IN | | The $\overline{RESET}$ pin is connected to the $\overline{RESET}$ pin on the register and to the $\overline{RESET}$ pin on the DRAM. When low, all register outputs will be driven low and the Clock Driver clocks to the DRAMs and register(s) will be set to low level (the Clock Driver will remain synchronized with the input clock) |
| Par_In | IN | | Parity bit for the Address and Control bus. ("1 " : Odd, "0 ": Even) |
| $\overline{Err\_Out}$ | OUT (open drain) | | Parity error detected on the Address and Control bus. A resistor may be connected from $\overline{Err\_Out}$ bus line to $V_{DD}$ on the system planar to act as a pull up. |
| TEST | | | Used by memory bus analysis tools (unused (NC) on memory DIMMs) |

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# 8. Pinout Comparison Based On Module Type

| Pin | RDIMM | | UDIMM | |
|---|---|---|---|---|
| | Signal | NOTE | Signal | NOTE |
| 48, 49 | $V_{TT}$ | Additional connection for Termination Voltage for Address/Command/Control/Clock nets. | NC | Not used on UDIMMs |
| 120, 240 | $V_{TT}$ | Termination Voltage for Address/Command/Control/Clock nets. | $V_{TT}$ | Termination Voltage for Address/Command/Control/Clock nets. |
| 53 | Err_$\overline{Out}$ | Connected to the register on all RDIMMs NC Not used on UDIMMs | NC | NC Not used on UDIMMs |
| 63 | NC | Not used on RDIMMs | CK1 | Used for 2 rank UDIMMs, not used on single-rank UDIMMs, but terminated |
| 64 | NC | | $\overline{CK1}$ | |
| 68 | Par_In | Connected to the register on all RDIMMs | NC | Not used on RDIMMs |
| 76 | $\overline{S}$1 | Connected to the register on all RDIMMs | $\overline{S}$1 | Used for dual-rank UDIMMs, not connected on single-rank UDIMMs |
| 77 | ODT1, NC | Connected to the register on dual- and quadrank RDIMMs; NC on single-rank RDIMMs | ODT1,NC | Used for dual-rank UDIMMs, not connected on single-rank UDIMMs |
| 79 | $\overline{S}$2, NC | Connected to the register on quad-rank RDIMMs, not connected on single or dual rank RDIMMs | NC | Not used on UDIMMs |
| 167 | NC | TEST input used only on bus analysis probes | NC | TEST input used only on bus analysis probes |
| 169 | CKE1 | Connected to the register on dual- and quadrank RDIMMs; NC on single-rank RDIMMs | CKE1, NC | Used for dual-rank UDIMMs, not connected on single-rank UDIMMs |
| 171 | A15 | Connected to the register on all RDIMMs | A15, NC | Depending on device density, may not be connected to SDRAMs on UDIMMs. However, these signals are terminated on UDIMMs. A15 not routed on some RCs |
| 172 | A14 | | A14 | |
| 196 | A13 | | A13 | |
| 198 | $\overline{S}$3, NC | Connected to the register on quad-rank RDIMMs, not connected on single-or dual-rank RDIMMs | NC | Not used on UDIMMs |
| 39, 40, 45, 46, 158, 159, 164, 165 | CBn | Used on all RDIMMs; (n = 0...7) | NC, CBn | Used on x72 UDIMMs, (n = 0...7); not used on x64 UDIMMs |
| 125, 134, 143, 152, 161, 203, 212, 221, 230 | DQSn, TDQSn | Connected to DQS on x4 SDRAMs, TDQS on x8 SDRAMs on RDIMMs; (n = 9...17) | DMn | Connected to DM on x8 DRAMs, UDM or LDM on x16 DRAMs on UDIMMs; (n = 0...8) |
| 126, 135, 144, 153, 162, 204, 213, 222, 231 | $\overline{DQS}$n, $\overline{TDQS}$n | Connected to $\overline{DQS}$ on x4 DRAMs, $\overline{TDQS}$ on x8 SDRAMs on RDIMMs; (n=9...17) | NC | Not used on UDIMMs |
| 187 | $\overline{EVENT}$ NC | Connected to optional thermal sensing component. NC on Modules without a thermal sensing component. | NC | Not used on UDIMMs |

**NOTE** : NC = No internal Connection

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# 9. Registering Clock Driver Specification

## 9.1 Timing & Capacitance values

| Symbol | Parameter | Conditions | $T_C$ = TBD, $V_{DD}$ = 1.5 ± 0.075V | | Units | Notes |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| fclock | Input Clock Frequency | application frequency | 300 | 670 | MHz | |
| $t_{CH}/t_{CL}$ | Pulse duration, CK, $\overline{CK}$ HIGH or LOW | | 0.4 | - | $t_{CK}$ | |
| $t_{ACT}$ | Inputs active time4 before RESET is taken HIGH | $\overline{DCKE0/1}$ = LOW and $\overline{DCS0/1}$ = HIGH | 8 | - | $t_{CK}$ | |
| $t_{SU}$ | Setup time | Input valid before CK/$\overline{CK}$ | 100 | - | ps | |
| $t_H$ | Hold time | Input to remain Valid after CK/$\overline{CK}$ | 175 | - | | |
| $t_{PDM}$ | Propagation delay, single-bit switching | CK/$\overline{CK}$ to output | 0.65 | 1.0 | ns | |
| $t_{DIS}$ | output disable time(1/2-Clock pre-launch) | CK/$\overline{CK}$ to output float | 0.5 | - | $t_{CK}$ | |
| | output disable time(3/4-Clock pre-launch) | | 0.25 | - | | |
| $t_{EN}$ | output enable time(1/2-Clock pre-launch) | CK/$\overline{CK}$ to output driving | - | 0.5 | $t_{CK}$ | |
| | output enable time(3/4-Clock pre-launch) | | - | 0.25 | | |
| $C_{IN}$(DATA) | Data Input Capacitance | | 1.5 | 2.5 | pF | |
| $C_{IN}$(CLOCK) | Data Input Capacitance | | 2 | 3 | | |
| $C_{IN}$(RST) | Reset Input Capacitance | | - | 3 | | |

## 9.2 Clock driver Characteristics

| Symbol | Parameter | Conditions | $T_C$ = TBD, $V_{DD}$ = 1.5 ± 0.075V | | Units | Notes |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| $t_{jit}$ (cc) | Cycle-to-cycle period jitter | | 0 | 40 | ps | |
| $t_{STAB}$ | Stabilization time | | - | 6 | us | |
| $t_{fdyn}$ | Dynamic phase offset | | -50 | 50 | ps | |
| $t_{CKsk}$ | Clock Output skew | | | 50 | ps | |
| $t_{jit}$(per) | Yn Clock Period jitter | | -40 | 40 | ps | |
| $t_{jit}$(hper) | Half period jitter | | -50 | 50 | ps | |
| $t_{Qsk1}$ | Qn Output to clock tolerance (Standard 1/2 -Clock Pre-Launch) | Output Inversion enabled | -100 | 200 | ps | |
| | | OUtput Inversion disabled | -100 | 300 | | |
| $t_{Qsk1}$ | Output clock tolerance (3/4 Clock Pre-Launch) | Output Inversion enabled | -100 | 200 | ps | |
| | | OUtput Inversion disabled | -100 | 300 | | |
| $t_{dynoff}$ | Maximum re-driven dynamic clock off-set | | -80 | 80 | ps | |

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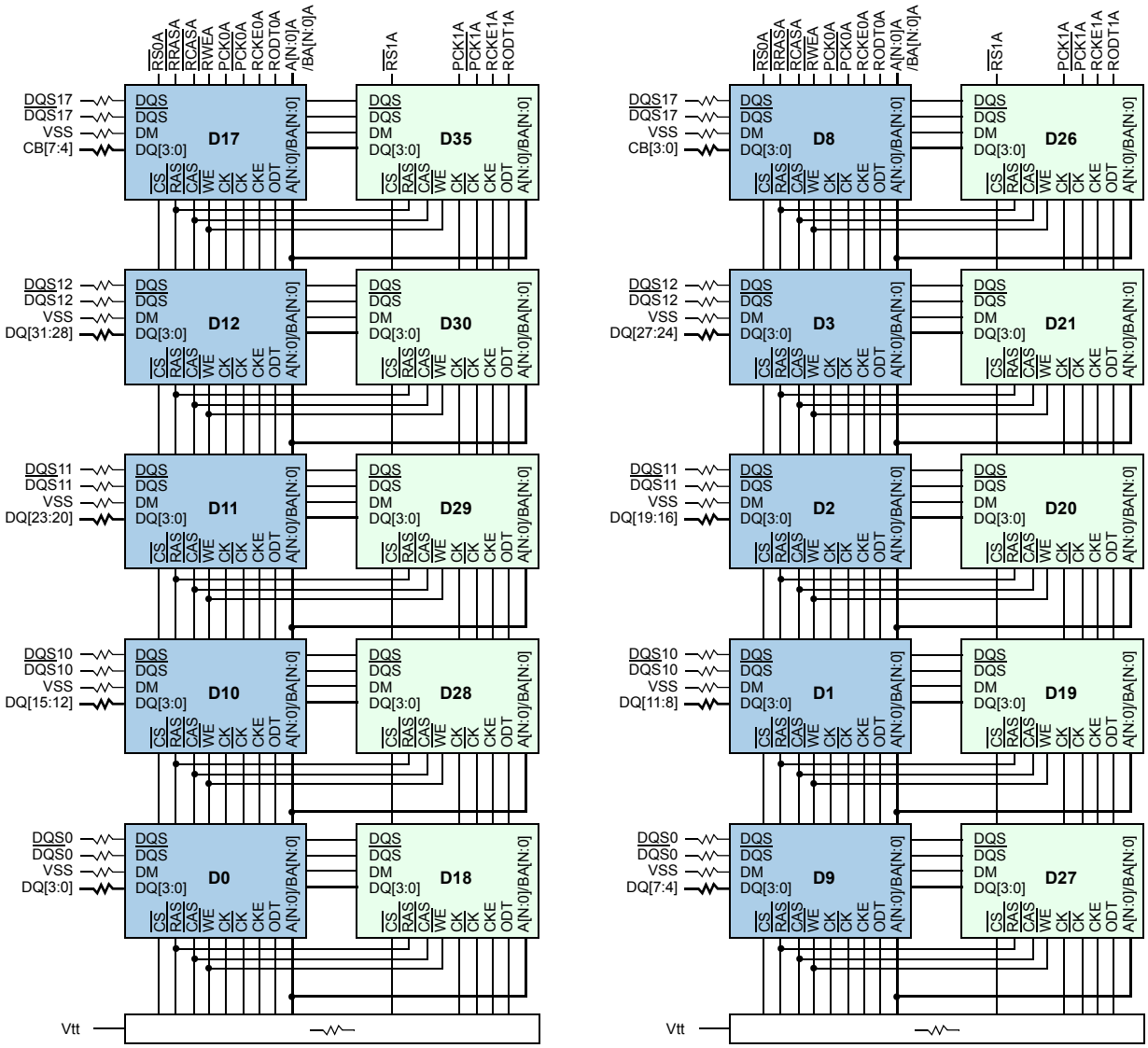
# 10. Function Block Diagram:

## 10.1 16GB, 2Gx72 Module (Populated as 2 ranks of x4 DDR3 SDRAMs)



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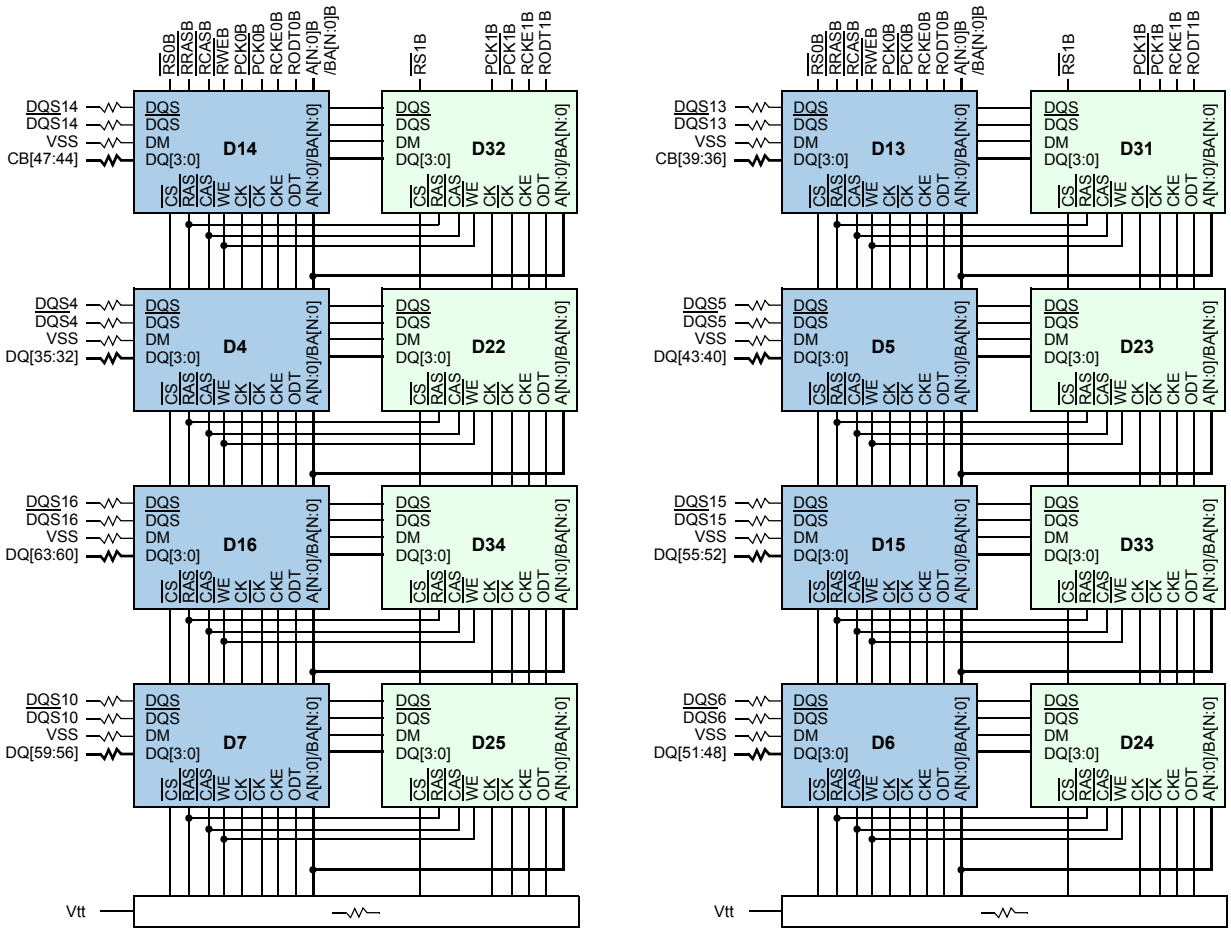
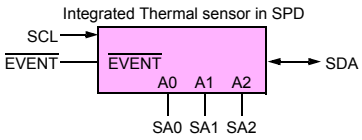
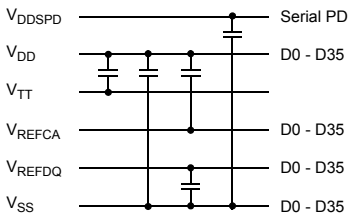
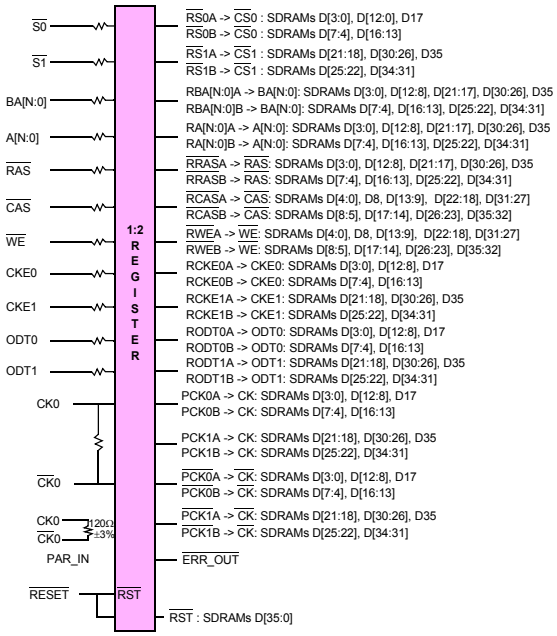



Serial PD w/ integrated Thermal sensor





S0
S1
BA[N:0]
A[N:0]
RAS
CAS
WE
CKE0
CKE1
ODT0
ODT1
CK0
CK0
CK0
CK0
120Ω ±3%
PAR_IN
RESET
1:2 REGISTER
RST
RS0A -> CS0 : SDRAMs D[3:0], D[12:0], D17
RS0B -> CS0 : SDRAMs D[7:4], D[16:13]
RS1A -> CS1 : SDRAMs D[21:18], D[30:26], D35
RS1B -> CS1 : SDRAMs D[25:22], D[34:31]
RBA[N:0]A -> BA[N:0]: SDRAMs D[3:0], D[12:8], D[21:17], D[30:26], D35
RBA[N:0]B -> BA[N:0]: SDRAMs D[7:4], D[16:13], D[25:22], D[34:31]
RA[N:0]A -> A[N:0]: SDRAMs D[3:0], D[12:8], D[21:17], D[30:26], D35
RA[N:0]B -> A[N:0]: SDRAMs D[7:4], D[16:13], D[25:22], D[34:31]
RRASA -> RAS: SDRAMs D[3:0], D[12:8], D[21:17], D[30:26], D35
RRASB -> RAS: SDRAMs D[7:4], D[16:13], D[25:22], D[34:31]
RCASA -> CAS: SDRAMs D[4:0], D8, D[13:9], D[22:18], D[31:27]
RCASB -> CAS: SDRAMs D[8:5], D[17:14], D[26:23], D[35:32]
RWEA -> WE: SDRAMs D[4:0], D8, D[13:9], D[22:18], D[31:27]
RWEB -> WE: SDRAMs D[8:5], D[17:14], D[26:23], D[35:32]
RCKE0A -> CKE0: SDRAMs D[3:0], D[12:8], D17
RCKE0B -> CKE0: SDRAMs D[7:4], D[16:13]
RCKE1A -> CKE1: SDRAMs D[21:18], D[30:26], D35
RCKE1B -> CKE1: SDRAMs D[25:22], D[34:31]
RODT0A -> ODT0: SDRAMs D[3:0], D[12:8], D17
RODT0B -> ODT0: SDRAMs D[7:4], D[16:13]
RODT1A -> ODT1: SDRAMs D[21:18], D[30:26], D35
RODT1B -> ODT1: SDRAMs D[25:22], D[34:31]
PCK0A -> CK: SDRAMs D[3:0], D[12:8], D17
PCK0B -> CK: SDRAMs D[7:4], D[16:13]
PCK1A -> CK: SDRAMs D[21:18], D[30:26], D35
PCK1B -> CK: SDRAMs D[25:22], D[34:31]
PCK0A -> CK: SDRAMs D[3:0], D[12:8], D17
PCK0B -> CK: SDRAMs D[7:4], D[16:13]
PCK1A -> CK: SDRAMs D[21:18], D[30:26], D35
PCK1B -> CK: SDRAMs D[25:22], D[34:31]
ERR_OUT
RST : SDRAMs D[35:0]

**NOTE**:
1. See wiring diagrams for resistor values.
2. ZQ pins of each SDRAM are connected to individual RZQ resistors (240 +/-1%)ohms...

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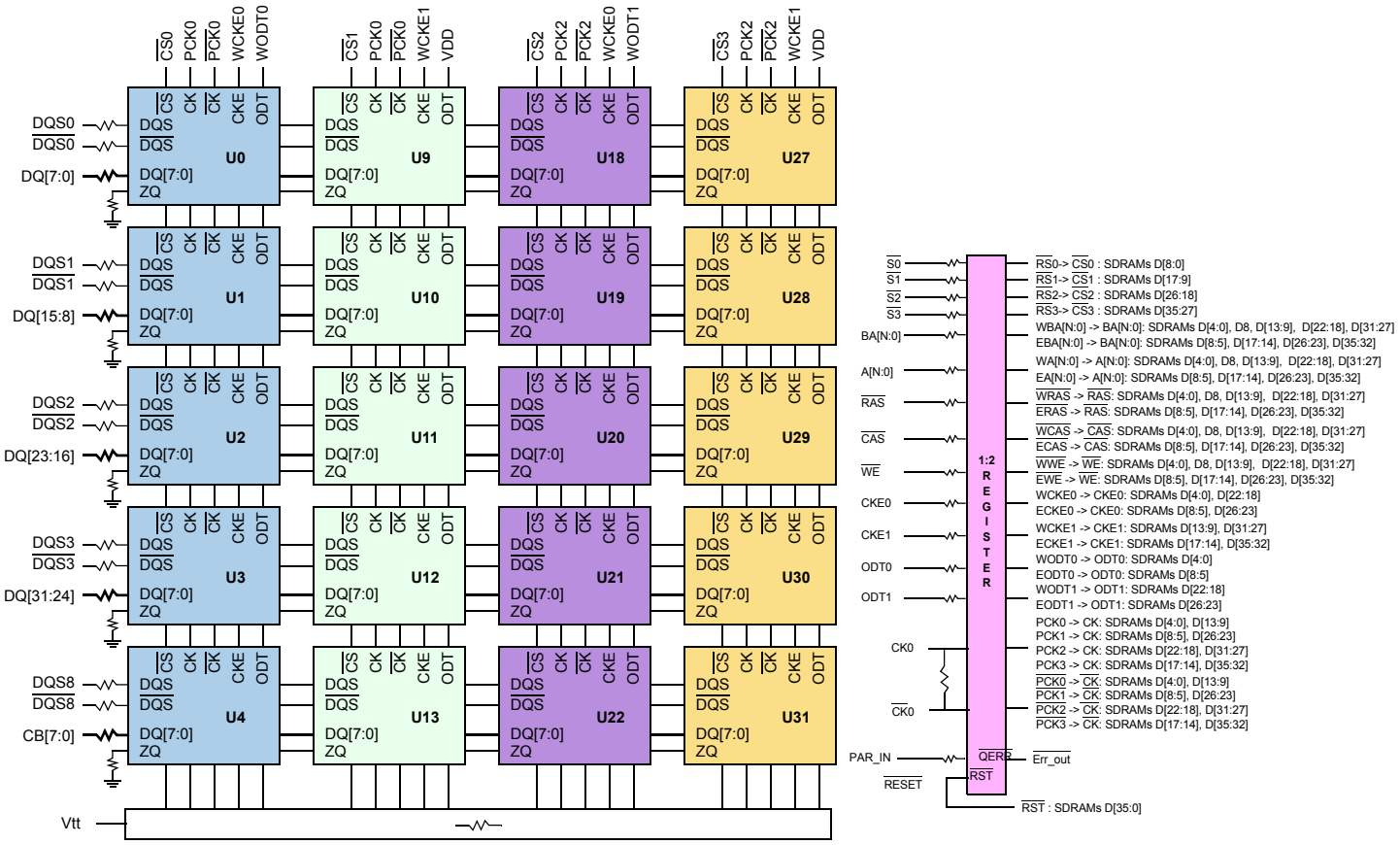
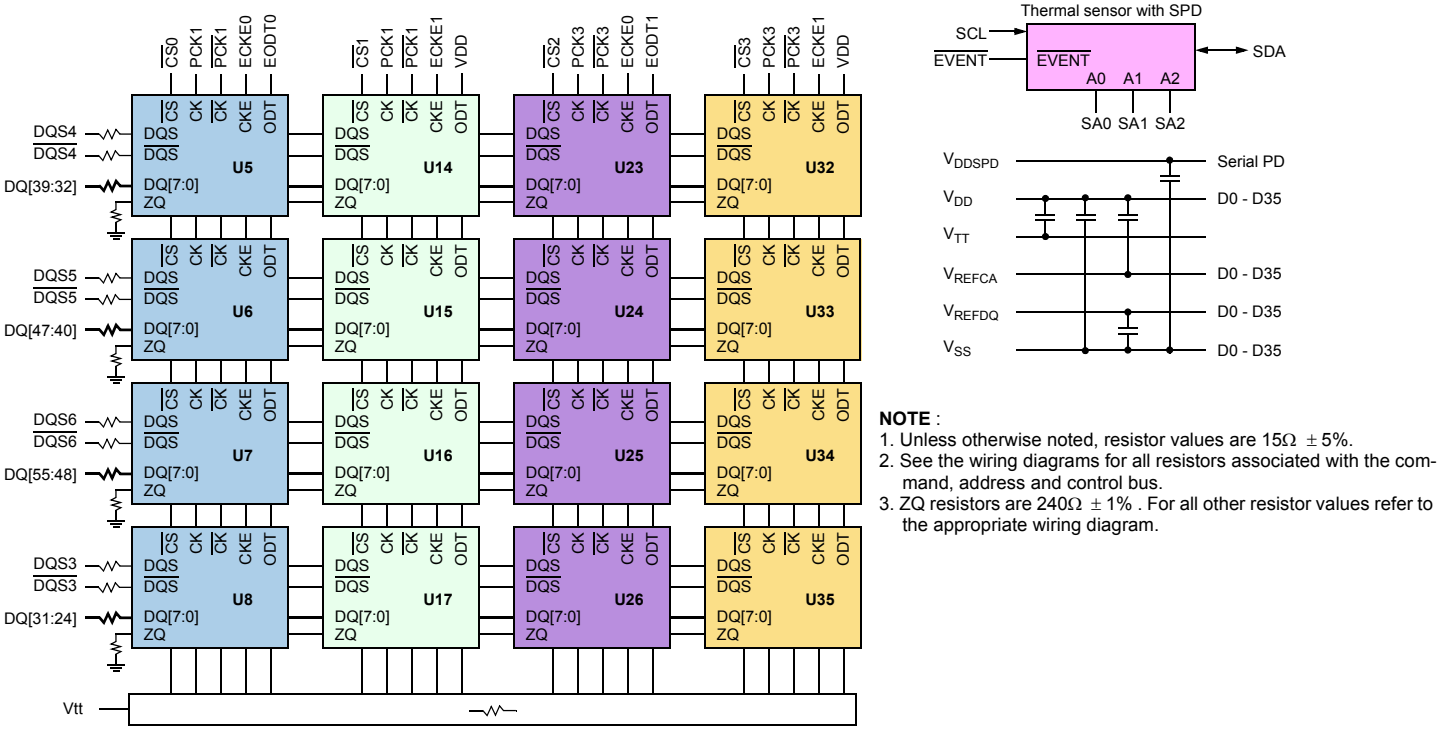
## 10.2 16GB, 2Gx72 Module (Populated as 4 ranks of x8 DDR3 SDRAMs)


CS0 PCK0 PCK0 WCKE0 WODT0
CS1 PCK0 PCK0 WCKE1 VDD
CS2 PCK2 PCK2 WCKE0 WODT1
CS3 PCK2 PCK2 WCKE1 VDD
DQS0 DQS0 DQ[7:0]
DQS1 DQS1 DQ[15:8]
DQS2 DQS2 DQ[23:16]
DQS3 DQS3 DQ[31:24]
DQS8 DQS8 CB[7:0]
U0 U9 U18 U27
U1 U10 U19 U28
U2 U11 U20 U29
U3 U12 U21 U30
U4 U13 U22 U31
Vtt
S0 S1 S2 S3
BA[N:0]
A[N:0]
RAS
CAS
WE
CKE0
CKE1
ODT0
ODT1
CK0
PAR_IN
RESET
1:2 REGISTER
QERR
RST
Err_out
RS0-> CS0 : SDRAMs D[8:0]
RS1-> CS1 : SDRAMs D[17:9]
RS2-> CS2 : SDRAMs D[26:18]
RS3-> CS3 : SDRAMs D[35:27]
WBA[N:0] -> BA[N:0]: SDRAMs D[4:0], D8, D[13:9], D[22:18], D[31:27]
EBA[N:0] -> BA[N:0]: SDRAMs D[8:5], D[17:14], D[26:23], D[35:32]
WA[N:0] -> A[N:0]: SDRAMs D[4:0], D8, D[13:9], D[22:18], D[31:27]
EA[N:0] -> A[N:0]: SDRAMs D[8:5], D[17:14], D[26:23], D[35:32]
WRAS -> RAS: SDRAMs D[4:0], D8, D[13:9], D[22:18], D[31:27]
ERAS -> RAS: SDRAMs D[8:5], D[17:14], D[26:23], D[35:32]
WCAS -> CAS: SDRAMs D[4:0], D8, D[13:9], D[22:18], D[31:27]
ECAS -> CAS: SDRAMs D[8:5], D[17:14], D[26:23], D[35:32]
WWE -> WE: SDRAMs D[4:0], D8, D[13:9], D[22:18], D[31:27]
EWE -> WE: SDRAMs D[8:5], D[17:14], D[26:23], D[35:32]
WCKE0 -> CKE0: SDRAMs D[4:0], D[22:18]
ECKE0 -> CKE0: SDRAMs D[8:5], D[26:23]
WCKE1 -> CKE1: SDRAMs D[13:9], D[31:27]
ECKE1 -> CKE1: SDRAMs D[17:14], D[35:32]
WODT0 -> ODT0: SDRAMs D[4:0]
EODT0 -> ODT0: SDRAMs D[8:5]
WODT1 -> ODT1: SDRAMs D[22:18]
EODT1 -> ODT1: SDRAMs D[26:23]
PCK0 -> CK: SDRAMs D[4:0], D[13:9]
PCK1 -> CK: SDRAMs D[8:5], D[26:23]
PCK2 -> CK: SDRAMs D[22:18], D[31:27]
PCK3 -> CK: SDRAMs D[17:14], D[35:32]
PCK0 -> CK: SDRAMs D[4:0], D[13:9]
PCK1 -> CK: SDRAMs D[8:5], D[26:23]
PCK2 -> CK: SDRAMs D[22:18], D[31:27]
PCK3 -> CK: SDRAMs D[17:14], D[35:32]
RST : SDRAMs D[35:0]







**NOTE** :
1. Unless otherwise noted, resistor values are 15Ω ±5%.
2. See the wiring diagrams for all resistors associated with the command, address and control bus.
3. ZQ resistors are 240Ω ±1% . For all other resistor values refer to the appropriate wiring diagram.

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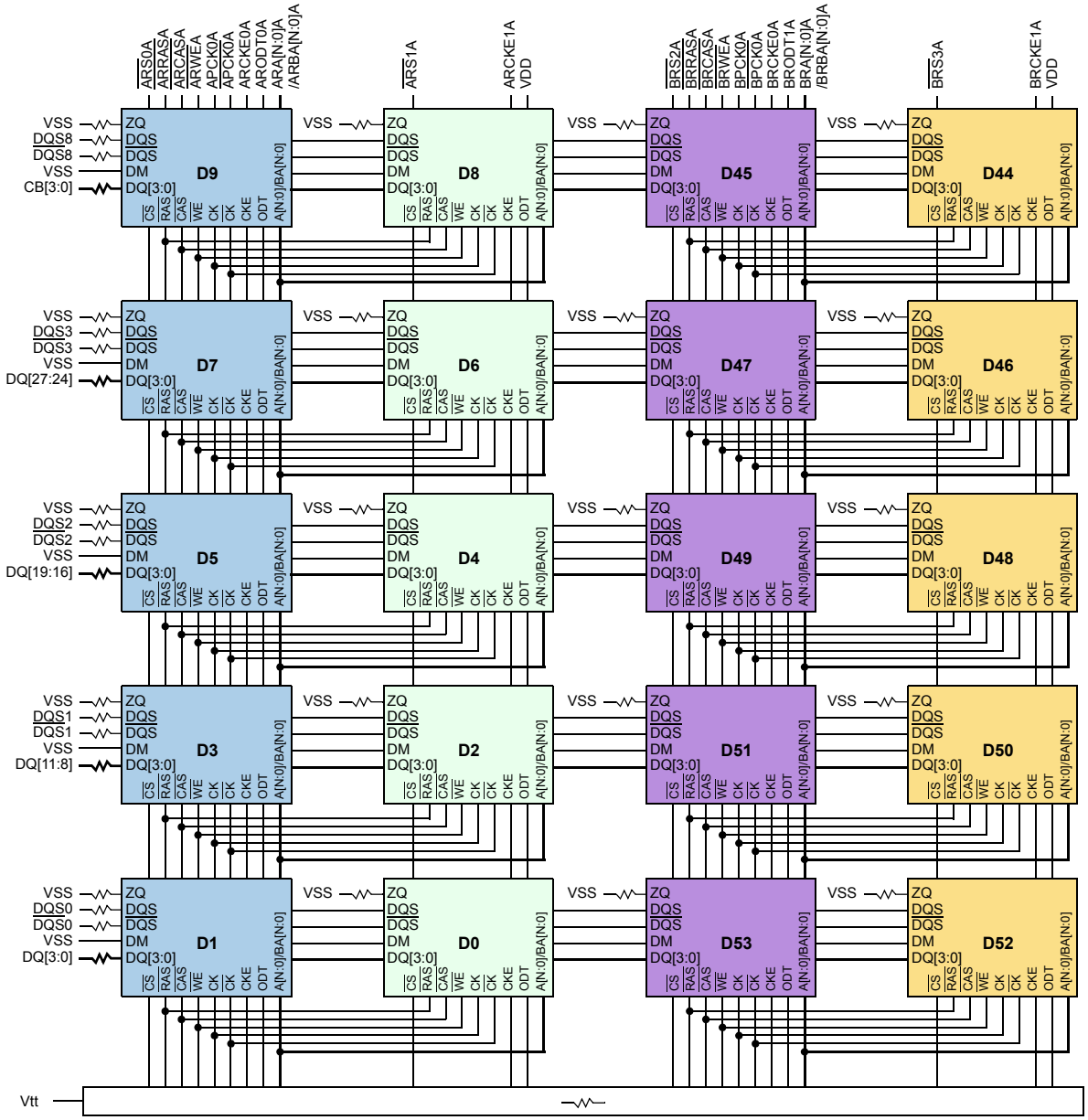
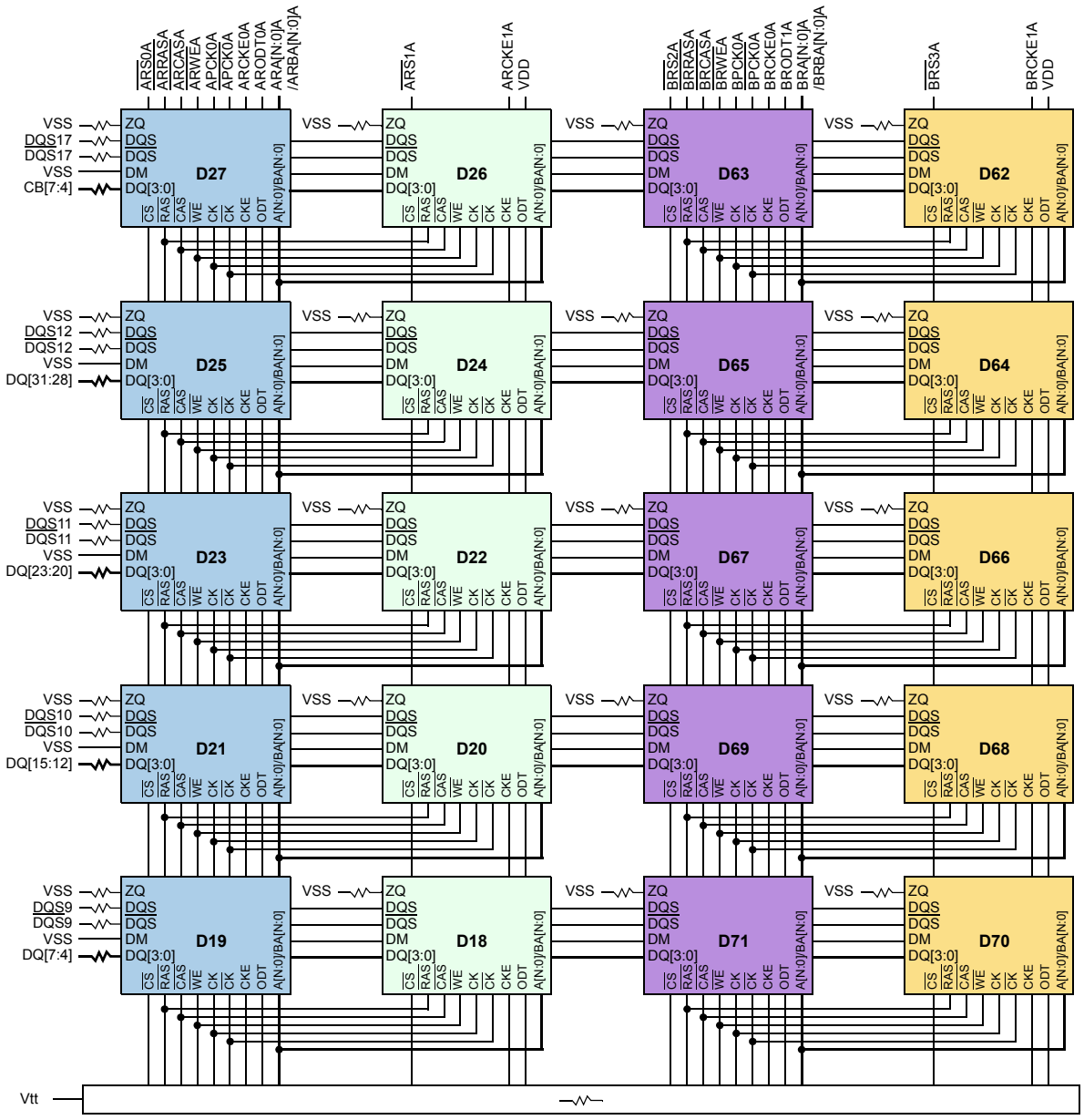
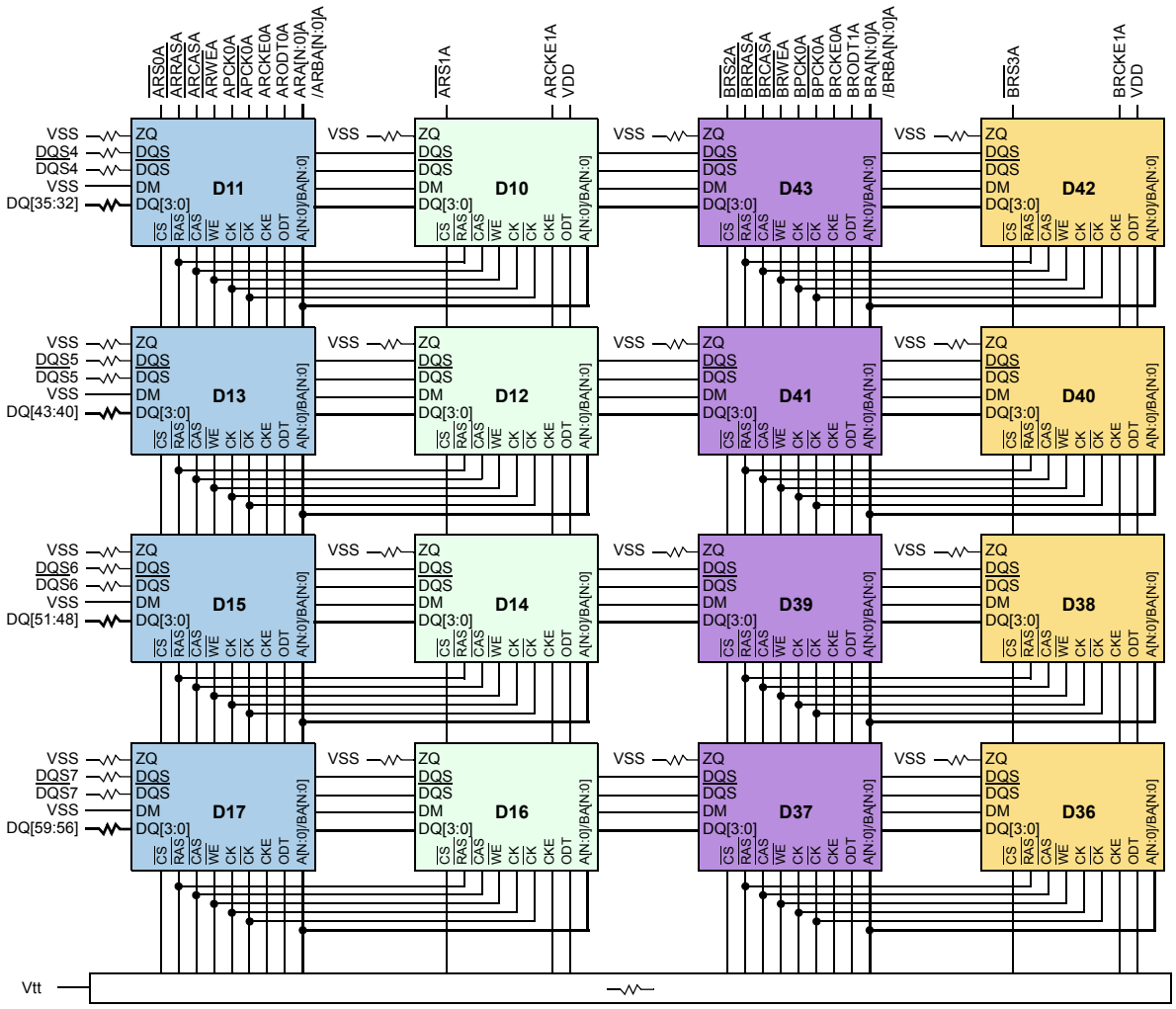
## 10.3 32GB, 4Gx72 Module (Populated as 4 ranks of x4 DDR3 SDRAMs)



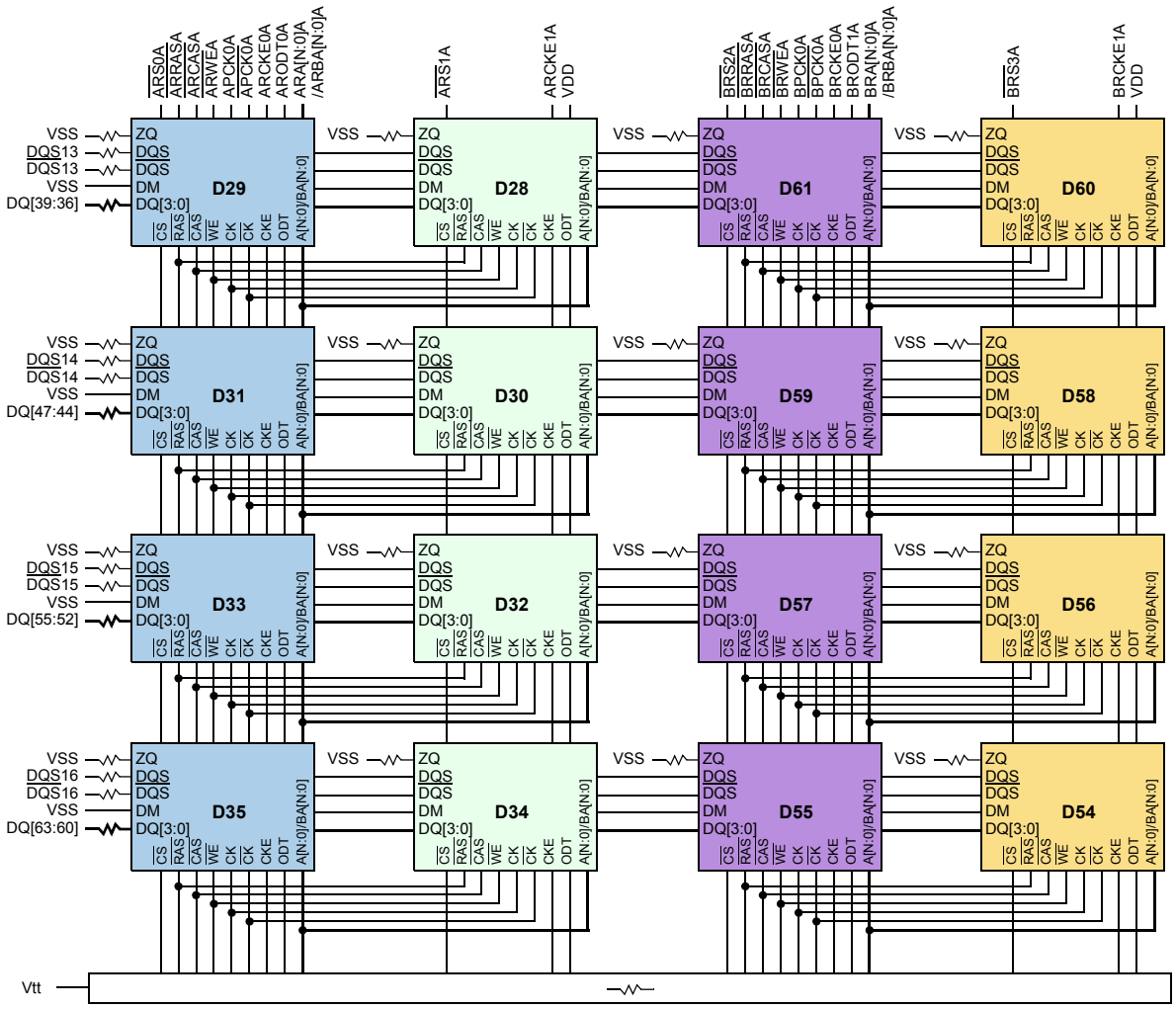
http://www.BDTIC.com/SAMSUNG
datasheet

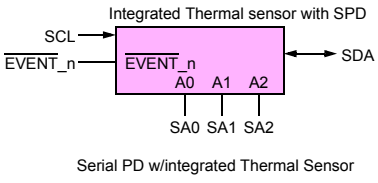



http://www.BDTIC.com/SAMSUNG
datasheet

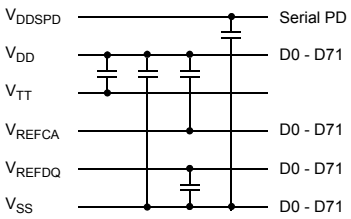



http://www.BDTIC.com/SAMSUNG
datasheet




Serial PD w/integrated Thermal Sensor




**NOTE** :
1. Unless otherwise noted, resistor values are 15Ω ± 5%.
2. See the wiring diagrams for all resistors associated with the command, address and control bus.
3. ZQ resistors are 240Ω ± 1%. For all other resistor values refer to the appropriate wiring diagram.

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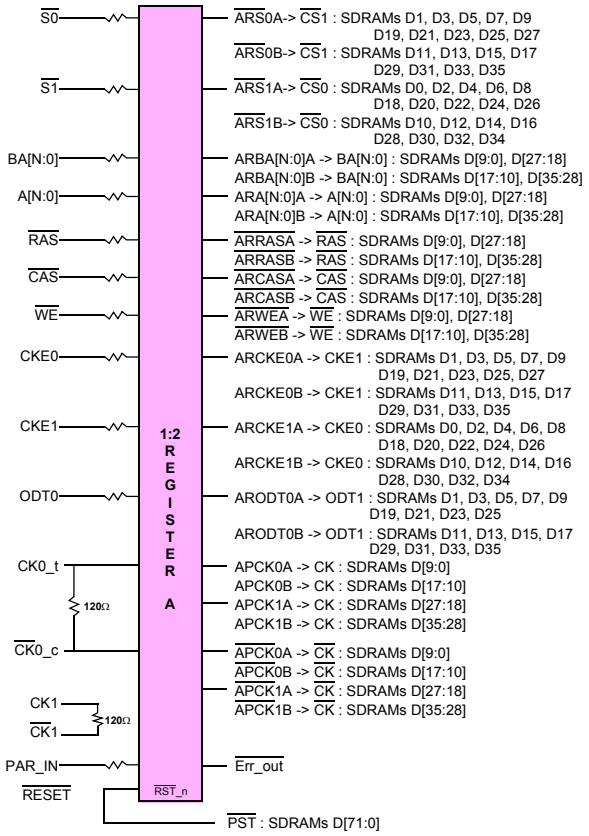
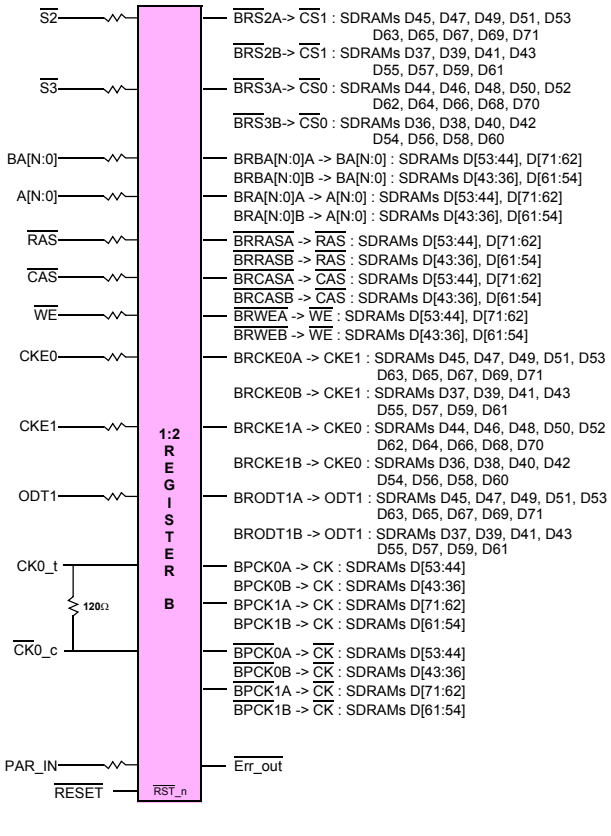

S0
S1
BA[N:0]
A[N:0]
RAS
CAS
WE
CKE0
CKE1
ODT0
CK0_t
120Ω
CK0_c
CK1
120Ω
CK1
PAR_IN
RESET
1:2 REGISTER A
RST_n
ARS0A-> CS1 : SDRAMs D1, D3, D5, D7, D9 D19, D21, D23, D25, D27
ARS0B-> CS1 : SDRAMs D11, D13, D15, D17 D29, D31, D33, D35
ARS1A-> CS0 : SDRAMs D0, D2, D4, D6, D8 D18, D20, D22, D24, D26
ARS1B-> CS0 : SDRAMs D10, D12, D14, D16 D28, D30, D32, D34
ARBA[N:0]A -> BA[N:0] : SDRAMs D[9:0], D[27:18]
ARBA[N:0]B -> BA[N:0] : SDRAMs D[17:10], D[35:28]
ARA[N:0]A -> A[N:0] : SDRAMs D[9:0], D[27:18]
ARA[N:0]B -> A[N:0] : SDRAMs D[17:10], D[35:28]
ARRASA -> RAS : SDRAMs D[9:0], D[27:18]
ARRASB -> RAS : SDRAMs D[17:10], D[35:28]
ARCASA -> CAS : SDRAMs D[9:0], D[27:18]
ARCASB -> CAS : SDRAMs D[17:10], D[35:28]
ARWEA -> WE : SDRAMs D[9:0], D[27:18]
ARWEB -> WE : SDRAMs D[17:10], D[35:28]
ARCKE0A -> CKE1 : SDRAMs D1, D3, D5, D7, D9 D19, D21, D23, D25, D27
ARCKE0B -> CKE1 : SDRAMs D11, D13, D15, D17 D29, D31, D33, D35
ARCKE1A -> CKE0 : SDRAMs D0, D2, D4, D6, D8 D18, D20, D22, D24, D26
ARCKE1B -> CKE0 : SDRAMs D10, D12, D14, D16 D28, D30, D32, D34
ARODT0A -> ODT1 : SDRAMs D1, D3, D5, D7, D9 D19, D21, D23, D25
ARODT0B -> ODT1 : SDRAMs D11, D13, D15, D17 D29, D31, D33, D35
APCK0A -> CK : SDRAMs D[9:0]
APCK0B -> CK : SDRAMs D[17:10]
APCK1A -> CK : SDRAMs D[27:18]
APCK1B -> CK : SDRAMs D[35:28]
APCK0A -> CK : SDRAMs D[9:0]
APCK0B -> CK : SDRAMs D[17:10]
APCK1A -> CK : SDRAMs D[27:18]
APCK1B -> CK : SDRAMs D[35:28]
Err_out
PST : SDRAMs D[71:0]


S2
S3
BA[N:0]
A[N:0]
RAS
CAS
WE
CKE0
CKE1
ODT1
CK0_t
120Ω
CK0_c
PAR_IN
RESET
1:2 REGISTER B
RST_n
BRS2A-> CS1 : SDRAMs D45, D47, D49, D51, D53 D63, D65, D67, D69, D71
BRS2B-> CS1 : SDRAMs D37, D39, D41, D43 D55, D57, D59, D61
BRS3A-> CS0 : SDRAMs D44, D46, D48, D50, D52 D62, D64, D66, D68, D70
BRS3B-> CS0 : SDRAMs D36, D38, D40, D42 D54, D56, D58, D60
BRBA[N:0]A -> BA[N:0] : SDRAMs D[53:44], D[71:62]
BRBA[N:0]B -> BA[N:0] : SDRAMs D[43:36], D[61:54]
BRA[N:0]A -> A[N:0] : SDRAMs D[53:44], D[71:62]
BRA[N:0]B -> A[N:0] : SDRAMs D[43:36], D[61:54]
BRRASA -> RAS : SDRAMs D[53:44], D[71:62]
BRRASB -> RAS : SDRAMs D[43:36], D[61:54]
BRCASA -> CAS : SDRAMs D[53:44], D[71:62]
BRCASB -> CAS : SDRAMs D[43:36], D[61:54]
BRWEA -> WE : SDRAMs D[53:44], D[71:62]
BRWEB -> WE : SDRAMs D[43:36], D[61:54]
BRCKE0A -> CKE1 : SDRAMs D45, D47, D49, D51, D53 D63, D65, D67, D69, D71
BRCKE0B -> CKE1 : SDRAMs D37, D39, D41, D43 D55, D57, D59, D61
BRCKE1A -> CKE0 : SDRAMs D44, D46, D48, D50, D52 D62, D64, D66, D68, D70
BRCKE1B -> CKE0 : SDRAMs D36, D38, D40, D42 D54, D56, D58, D60
BRODT1A -> ODT1 : SDRAMs D45, D47, D49, D51, D53 D63, D65, D67, D69, D71
BRODT1B -> ODT1 : SDRAMs D37, D39, D41, D43 D55, D57, D59, D61
BPCK0A -> CK : SDRAMs D[53:44]
BPCK0B -> CK : SDRAMs D[43:36]
BPCK1A -> CK : SDRAMs D[71:62]
BPCK1B -> CK : SDRAMs D[61:54]
BPCK0A -> CK : SDRAMs D[53:44]
BPCK0B -> CK : SDRAMs D[43:36]
BPCK1A -> CK : SDRAMs D[71:62]
BPCK1B -> CK : SDRAMs D[61:54]
Err_out

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# 11. Absolute Maximum Ratings

## 11.1 Absolute Maximum DC Ratings

| Symbol | Parameter | Rating | Units | NOTE |
|---|---|---|---|---|
| $V_{DD}$ | Voltage on $V_{DD}$ pin relative to $V_{SS}$ | -0.4 V ~ 1.975 V | V | 1,3 |
| $V_{DDQ}$ | Voltage on $V_{DDQ}$ pin relative to $V_{SS}$ | -0.4 V ~ 1.975 V | V | 1,3 |
| $V_{IN}$, $V_{OUT}$ | Voltage on any pin relative to $V_{SS}$ | -0.4 V ~ 1.975 V | V | 1 |
| $T_{STG}$ | Storage Temperature | -55 to +100 | °C | 1, 2 |

**NOTE** :
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. $V_{DD}$ and $V_{DDQ}$ must be within 300mV of each other at all times; and $V_{REF}$ must be not greater than 0.6 x $V_{DDQ}$, When $V_{DD}$ and $V_{DDQ}$ are less than 500mV; $V_{REF}$ may be equal to or less than 300mV.

## 11.2 DRAM Component Operating Temperature Range

| Symbol | Parameter | rating | Unit | NOTE |
|---|---|---|---|---|
| $T_{OPER}$ | Operating Temperature Range | 0 to 95 | °C | 1, 2, 3 |

**NOTE** :
1. Operating Temperature $T_{OPER}$ is the case surface temperature on the center/top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85°C under all operating conditions
3. Some applications require operation of the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us. It is also possible to specify a component with 1X refresh (tREFI to 7.8us) in the Extended Temperature Range.
   b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b), in this case IDD6 current can be increased around 10~20% than normal Temperature range.

# 12. AC & DC Operating Conditions

## 12.1 Recommended DC Operating Conditions (SSTL-15)

| Symbol | Parameter | Rating | | | Units | NOTE |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $V_{DD}$ | Supply Voltage | 1.425 | 1.5 | 1.575 | V | 1,2 |
| $V_{DDQ}$ | Supply Voltage for Output | 1.425 | 1.5 | 1.575 | V | 1,2 |

**NOTE**:
1. Under all conditions $V_{DDQ}$ must be less than or equal to $V_{DD}$.
2. $V_{DDQ}$ tracks with $V_{DD}$. AC parameters are measured with $V_{DD}$ and $V_{DDQ}$ tied together.

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# 13. AC & DC Input Measurement Levels

## 13.1 AC & DC Logic Input Levels for Single-ended Signals

**[ Table 2 ] Single Ended AC and DC input levels for Command and Address**

| Symbol | Parameter | DDR3-800/1066/1333/1600 | | Unit | NOTE |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| $V_{IH.CA}$(DC100) | DC input logic high | $V_{REF}$ + 100 | $V_{DD}$ | mV | 1,5 |
| $V_{IL.CA}$(DC100) | DC input logic low | $V_{SS}$ | $V_{REF}$ - 100 | mV | 1,6 |
| $V_{IH.CA}$(AC175) | AC input logic high | $V_{REF}$ + 175 | NOTE 2 | mV | 1,2,7 |
| $V_{IL.CA}$(AC175) | AC input logic low | NOTE 2 | $V_{REF}$ - 175 | mV | 1,2,8 |
| $V_{IH.CA}$(AC150) | AC input logic high | $V_{REF}$+150 | NOTE 2 | mV | 1,2,7 |
| $V_{IL.CA}$(AC150) | AC input logic low | NOTE 2 | $V_{REF}$-150 | mV | 1,2,8 |
| $V_{REFCA}$(DC) | Reference Voltage for ADD, CMD inputs | 0.49*$V_{DD}$ | 0.51*$V_{DD}$ | V | 3,4 |

**NOTE** :
1. For input only pins except $\overline{RESET}$, $V_{REF}$ = $V_{REFCA}$(DC)
2. See 'Overshoot/Undershoot Specification' on page 18.
3. The AC peak noise on $V_{REF}$ may not allow $V_{REF}$ to deviate from $V_{REF}$(DC) by more than ± 1% $V_{DD}$ (for reference : approx. ± 15mV)
4. For reference : approx. $V_{DD}$/2 ± 15mV
5. $V_{IH}$(dc) is used as a simplified symbol for $V_{IH.CA}$(DC100)
6. $V_{IL}$(dc) is used as a simplified symbol for $V_{IL.CA}$(DC100)
7. $V_{IH}$(ac) is used as a simplified symbol for $V_{IH.CA}$(AC175) and $V_{IH.CA}$(AC150); $V_{IH.CA}$(AC175) value is used when $V_{REF}$ + 175mV is referenced and $V_{IH.CA}$(AC150) value is used when VREF + 150mV is referenced.
8. $V_{IL}$(ac) is used as a simplified symbol for $V_{IL.CA}$(AC175) and $V_{IL.CA}$(AC150); $V_{IL.CA}$(AC175) value is used when $V_{REF}$ - 175mV is referenced and $V_{IL.CA}$(AC150) value is used when $V_{REF}$ - 150mV is referenced.

**[ Table 3 ] Single Ended AC and DC input levels for DQ and DM**

| Symbol | Parameter | DDR3-800/1066 | | DDR3-1333/1600 | | Unit | NOTE |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $V_{IH.DQ}$(DC100) | DC input logic high | $V_{REF}$ + 100 | $V_{DD}$ | $V_{REF}$ + 100 | $V_{DD}$ | mV | 1,5 |
| $V_{IL.DQ}$(DC100) | DC input logic low | $V_{SS}$ | $V_{REF}$ - 100 | $V_{SS}$ | $V_{REF}$ - 100 | mV | 1,6 |
| $V_{IH.DQ}$(AC175) | AC input logic high | $V_{REF}$ + 175 | NOTE 2 | - | - | mV | 1,2,7 |
| $V_{IL.DQ}$(AC175) | AC input logic low | NOTE 2 | $V_{REF}$ - 175 | - | - | mV | 1,2,8 |
| $V_{IH.DQ}$(AC150) | AC input logic high | $V_{REF}$ + 150 | NOTE 2 | $V_{REF}$ + 150 | NOTE 2 | mV | 1,2,7 |
| $V_{IL.DQ}$(AC150) | AC input logic low | NOTE 2 | $V_{REF}$ - 150 | NOTE 2 | $V_{REF}$ - 150 | mV | 1,2,8 |
| $V_{REFDQ}$(DC) | Reference Voltage for DQ, DM inputs | 0.49*$V_{DD}$ | 0.51*$V_{DD}$ | 0.49*$V_{DD}$ | 0.51*$V_{DD}$ | V | 3,4 |

**NOTE** :
1. For input only pins except $\overline{RESET}$, $V_{REF}$ = $V_{REFDQ}$(DC)
2. See 'Overshoot/Undershoot Specification' on page 18.
3. The AC peak noise on $V_{REF}$ may not allow $V_{REF}$ to deviate from $V_{REF}$(DC) by more than ± 1% $V_{DD}$ (for reference : approx. ± 15mV)
4. For reference : approx. $V_{DD}$/2 ± 15mV
5. $V_{IH}$(dc) is used as a simplified symbol for $V_{IH.DQ}$(DC100)
6. $V_{IL}$(dc) is used as a simplified symbol for $V_{IL.DQ}$(DC100)
7. $V_{IH}$(ac) is used as a simplified symbol for $V_{IH.DQ}$(AC175), $V_{IH.DQ}$(AC150) ; $V_{IH.DQ}$(AC175) value is used when $V_{REF}$ + 175mV is referenced, $V_{IH.DQ}$(AC150) value is used when $V_{REF}$ + 150mV is referenced.
8. $V_{IL}$(ac) is used as a simplified symbol for $V_{IL.DQ}$(AC175), $V_{IL.DQ}$(AC150) ; $V_{IL.DQ}$(AC175) value is used when $V_{REF}$ - 175mV is referenced, $V_{IL.DQ}$(AC150) value is used when $V_{REF}$ - 150mV is referenced.

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## 13.2 $V_{REF}$ Tolerances.

The dc-tolerance limits and ac-noise limits for the reference voltages $V_{REFCA}$ and $V_{REFDQ}$ are illustrate in Figure 1. It shows a valid reference voltage $V_{REF}(t)$ as a function of time. ($V_{REF}$ stands for $V_{REFCA}$ and $V_{REFDQ}$ likewise).

$V_{REF}(DC)$ is the linear average of $V_{REF}(t)$ over a very long period of time (e.g. 1 sec). This average has to meet the min/max requirements of $V_{REF}$. Furthermore $V_{REF}(t)$ may temporarily deviate from $V_{REF}(DC)$ by no more than ± 1% $V_{DD}$.

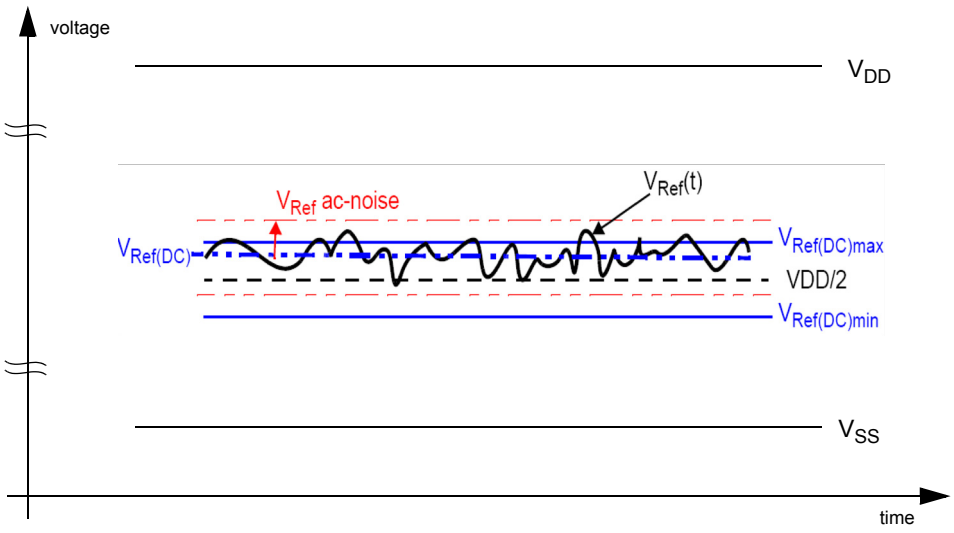


**Figure 1. Illustration of VREF(DC) tolerance and VREF ac-noise limits**

The voltage levels for setup and hold time measurements $V_{IH}(AC)$, $V_{IH}(DC)$, $V_{IL}(AC)$ and $V_{IL}(DC)$ are dependent on $V_{REF}$.

"$V_{REF}$" shall be understood as $V_{REF}(DC)$, as defined in Figure 1.

This clarifies, that dc-variations of $V_{REF}$ affect the absolute voltage a signal has to reach to achieve a valid high or low level and therefore the time to which setup and hold is measured. System timing and voltage budgets need to account for $V_{REF}(DC)$ deviations from the optimum position within the data-eye of the input signals.

This also clarifies that the DRAM setup/hold specification and derating values need to include time and voltage associated with $V_{REF}$ ac-noise.
Timing and voltage effects due to ac-noise on $V_{REF}$ up to the specified limit (+/-1% of $V_{DD}$) are included in DRAM timings and their associated deratings.

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## 13.3 AC and DC Logic Input Levels for Differential Signals

### 13.3.1 Differential Signals Definition

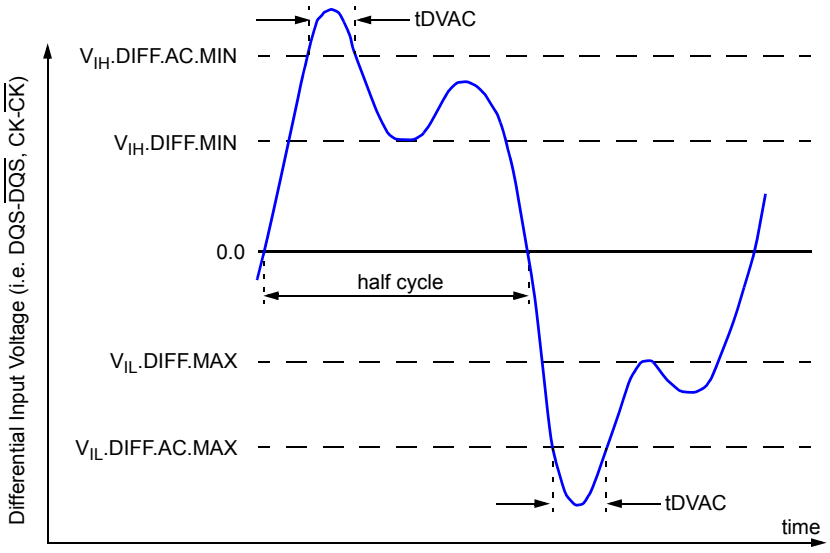


**Figure 2. Definition of differential ac-swing and "time above ac level" tDVAC**

### 13.3.2 Differential Swing Requirement for Clock (CK - $\overline{CK}$) and Strobe (DQS - $\overline{DQS}$)

| Symbol | Parameter | DDR3-800/1066/1333/1600 | | unit | NOTE |
|---|---|---|---|---|---|
| | | min | max | | |
| $V_{IHdiff}$ | differential input high | +0.2 | NOTE 3 | V | 1 |
| $V_{ILdiff}$ | differential input low | NOTE 3 | -0.2 | V | 1 |
| $V_{IHdiff}$(AC) | differential input high ac | 2 x ($V_{IH}$(AC) - $V_{REF}$) | NOTE 3 | V | 2 |
| $V_{ILdiff}$(AC) | differential input low ac | NOTE 3 | 2 x ($V_{IL}$(AC) - $V_{REF}$) | V | 2 |

**NOTE** :
1. Used to define a differential signal slew-rate.
2. for CK - $\overline{CK}$ use $V_{IH}/V_{IL}$(AC) of ADD/CMD and $V_{REFCA}$; for DQS - $\overline{DQS}$ use $V_{IH}/V_{IL}$(AC) of DQs and $V_{REFDQ}$; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
3. These values are not defined, however they single-ended signals CK, $\overline{CK}$, DQS, $\overline{DQS}$, DQSL need to be within the respective limits ($V_{IH}$(DC) max, $V_{IL}$(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "overshoot and Undersheet Specification"

**[ Table 4 ] Allowed time before ringback (tDVAC) for CK - $\overline{CK}$ and DQS - $\overline{DQS}$.**

| Slew Rate [V/ns] | tDVAC [ps] @ $\|V_{IH/Ldiff}(AC)\|$ = 350mV | | tDVAC [ps] @ $\|V_{IH/Ldiff}(AC)\|$ = 300mV | |
|---|---|---|---|---|
| | min | max | min | max |
| > 4.0 | 75 | - | 175 | - |
| 4.0 | 57 | - | 170 | - |
| 3.0 | 50 | - | 167 | - |
| 2.0 | 38 | - | 163 | - |
| 1.8 | 34 | - | 162 | - |
| 1.6 | 29 | - | 161 | - |
| 1.4 | 22 | - | 159 | - |
| 1.2 | 13 | - | 155 | - |
| 1.0 | 0 | - | 150 | - |
| < 1.0 | 0 | - | 150 | - |

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### 13.3.3 Single-ended Requirements for Differential Signals

Each individual component of a differential signal (CK, DQS, $\overline{CK}$, $\overline{DQS}$) has also to comply with certain requirements for single-ended signals.
CK and $\overline{CK}$ have to approximately reach $V_{SEH}$min / $V_{SEL}$max (approximately equal to the ac-levels ( $V_{IH}$(AC) / $V_{IL}$(AC) ) for ADD/CMD signals) in every half-cycle.
DQS, $\overline{DQS}$ have to reach $V_{SEH}$min / $V_{SEL}$max (approximately the ac-levels ( $V_{IH}$(AC) / $V_{IL}$(AC) ) for DQ signals) in every half-cycle proceeding and following a valid transition.
Note that the applicable ac-levels for ADD/CMD and DQ's might be different per speed-bin etc. E.g. if $V_{IH}$150(AC)/$V_{IL}$150(AC) is used for ADD/CMD signals, then these ac-levels apply also for the single-ended signals CK and $\overline{CK}$ .

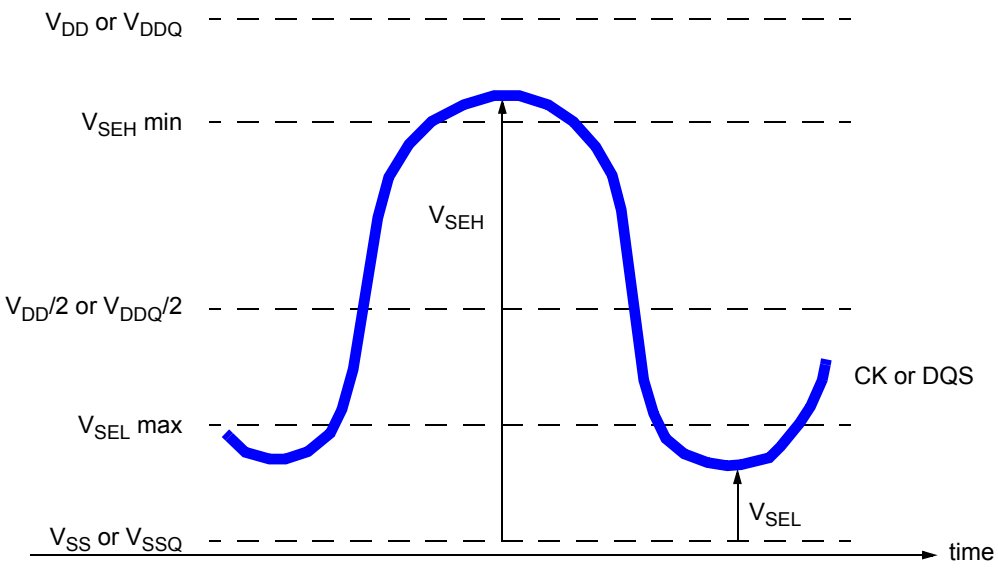


**Figure 3. Single-ended requirement for differential signals**

Note that while ADD/CMD and DQ signal requirements are with respect to $V_{REF}$, the single-ended components of differential signals have a requirement with respect to $V_{DD}$/2; this is nominally the same. The transition of single-ended signals through the ac-levels is used to measure setup time. For single-ended components of differential signals the requirement to reach $V_{SEL}$max, $V_{SEH}$min has no bearing on timing, but adds a restriction on the common mode characteristics of these signals.

**[ Table 5 ] Single ended levels for CK, DQS, $\overline{CK}$, $\overline{DQS}$**

| Symbol | Parameter | DDR3-800/1066/1333/1600 | | Unit | NOTE |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $V_{SEH}$ | Single-ended high-level for strobes | ($V_{DD}$/2)+0.175 | NOTE 3 | V | 1, 2 |
| | Single-ended high-level for CK, $\overline{CK}$ | ($V_{DD}$/2)+0.175 | NOTE 3 | V | 1, 2 |
| $V_{SEL}$ | Single-ended low-level for strobes | NOTE 3 | ($V_{DD}$/2)-0.175 | V | 1, 2 |
| | Single-ended low-level for CK, $\overline{CK}$ | NOTE 3 | ($V_{DD}$/2)-0.175 | V | 1, 2 |

**NOTE** :
1. For CK, $\overline{CK}$ use $V_{IH}$/$V_{IL}$(AC) of ADD/CMD; for strobes (DQS, $\overline{DQS}$) use $V_{IH}$/$V_{IL}$(AC) of DQs.
2. $V_{IH}$(AC)/$V_{IL}$(AC) for DQs is based on $V_{REFDQ}$; $V_{IH}$(AC)/$V_{IL}$(AC) for ADD/CMD is based on $V_{REFCA}$; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here
3. These values are not defined, however the single-ended signals CK, $\overline{CK}$, DQS, $\overline{DQS}$ need to be within the respective limits ($V_{IH}$(DC) max, $V_{IL}$(DC)min) for single-ended signals as well as the limitations for overshoot and undershoot. Refer to "Overshoot and Undershoot Specification"

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### 13.3.4 Differential Input Cross Point Voltage

To guarantee tight setup and hold times as well as output skew parameters with respect to clock and strobe, each cross point voltage of differential input signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) must meet the requirements in below table. The differential input cross point voltage $V_{IX}$ is measured from the actual cross point of true and complement signal to the mid level between of $V_{DD}$ and $V_{SS}$.

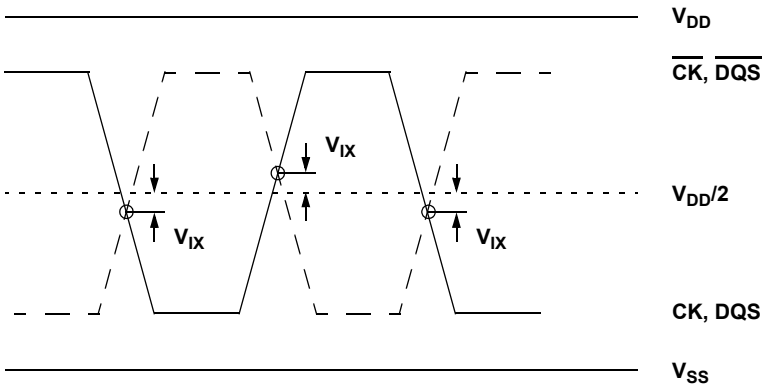


**Figure 4. $V_{IX}$ Definition**

**[ Table 6 ] Cross point voltage for differential input signals (CK, DQS)**

| Symbol | Parameter | DDR3-800/1066/1333/1600 | | Unit | NOTE |
|---|---|---|---|---|---|
| | | Min | Max | | |
| $V_{IX}$ | Differential Input Cross Point Voltage relative to $V_{DD}/2$ for CK,$\overline{CK}$ | -150 | 150 | mV | |
| | | -175 | 175 | mV | 1 |
| $V_{IX}$ | Differential Input Cross Point Voltage relative to $V_{DD}/2$ for DQS,$\overline{DQS}$ | -150 | 150 | mV | |

**NOTE** :
1. Extended range for $V_{IX}$ is only allowed for clock and if single-ended clock input signals CK and $\overline{CK}$ are monotonic, have a single-ended swing $V_{SEL}$ / $V_{SEH}$ of at least $V_{DD}/2$ ±250 mV, and the differential slew rate of CK-$\overline{CK}$ is larger than 3 V/ ns.

## 13.4 Slew Rate Definition for Single Ended Input Signals

See "Address / Command Setup, Hold and Derating" for single-ended slew rate definitions for address and command signals.
See "Data Setup, Hold and Slew Rate Derating" for single-ended slew rate definitions for data signals.

## 13.5 Slew rate definition for Differential Input Signals

Input slew rate for differential signals (CK, $\overline{CK}$ and DQS, $\overline{DQS}$) are defined and measured as shown in below.

**[ Table 7 ] Differential input slew rate definition**

| Description | Measured | | Defined by |
|---|---|---|---|
| | From | To | |
| Differential input slew rate for rising edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$) | $V_{ILdiffmax}$ | $V_{IHdiffmin}$ | $\frac{V_{IHdiffmin} - V_{ILdiffmax}}{\text{Delta TRdiff}}$ |
| Differential input slew rate for falling edge (CK-$\overline{CK}$ and DQS-$\overline{DQS}$) | $V_{IHdiffmin}$ | $V_{ILdiffmax}$ | $\frac{V_{IHdiffmin} - V_{ILdiffmax}}{\text{Delta TFdiff}}$ |

**NOTE** : The differential signal (i.e. CK - $\overline{CK}$ and DQS - $\overline{DQS}$) must be linear between these thresholds

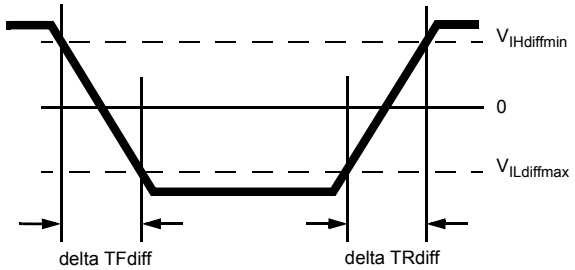


**Figure 5. Differential input slew rate definition for DQS, $\overline{DQS}$ and CK, $\overline{CK}$**

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# 14. AC & DC Output Measurement Levels

## 14.1 Single Ended AC and DC Output Levels

**[ Table 8 ] Single Ended AC and DC output levels**

| Symbol | Parameter | DDR3-800/1066/1333/1600 | Units | NOTE |
|---|---|---|---|---|
| $V_{OH}$(DC) | DC output high measurement level (for IV curve linearity) | 0.8 x $V_{DDQ}$ | V | |
| $V_{OM}$(DC) | DC output mid measurement level (for IV curve linearity) | 0.5 x $V_{DDQ}$ | V | |
| $V_{OL}$(DC) | DC output low measurement level (for IV curve linearity) | 0.2 x $V_{DDQ}$ | V | |
| $V_{OH}$(AC) | AC output high measurement level (for output SR) | $V_{TT}$ + 0.1 x $V_{DDQ}$ | V | 1 |
| $V_{OL}$(AC) | AC output low measurement level (for output SR) | $V_{TT}$ - 0.1 x $V_{DDQ}$ | V | 1 |

**NOTE** : 1. The swing of +/-0.1 x $V_{DDQ}$ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to $V_{TT}$=$V_{DDQ}$/2.

## 14.2 Differential AC and DC Output Levels

**[ Table 9 ] Differential AC and DC output levels**

| Symbol | Parameter | DDR3-800/1066/1333/1600 | Units | NOTE |
|---|---|---|---|---|
| $V_{OHdiff}$(AC) | AC differential output high measurement level (for output SR) | +0.2 x $V_{DDQ}$ | V | 1 |
| $V_{OLdiff}$(AC) | AC differential output low measurement level (for output SR) | -0.2 x $V_{DDQ}$ | V | 1 |

**NOTE** : 1. The swing of +/-0.2x$V_{DDQ}$ is based on approximately 50% of the static single ended output high or low swing with a driver impedance of 40Ω and an effective test load of 25Ω to $V_{TT}$=$V_{DDQ}$/2 at each of the differential outputs.

## 14.3 Single-ended Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OL}$(AC) and $V_{OH}$(AC) for single ended signals as shown in below.

**[ Table 10 ] Single ended Output slew rate definition**

| Description | Measured | | Defined by |
|---|---|---|---|
| | From | To | |
| Single ended output slew rate for rising edge | $V_{OL}$(AC) | $V_{OH}$(AC) | $\frac{V_{OH}(AC)-V_{OL}(AC)}{\text{Delta TRse}}$ |
| Single ended output slew rate for falling edge | $V_{OH}$(AC) | $V_{OL}$(AC) | $\frac{V_{OH}(AC)-V_{OL}(AC)}{\text{Delta TFse}}$ |

**NOTE** : Output slew rate is verified by design and characterization, and may not be subject to production test.

**[ Table 11 ] Single ended output slew rate**

| Parameter | Symbol | DDR3-800 | | DDR3-1066 | | DDR3-1333 | | DDR3-1600 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Single ended output slew rate | SRQse | 2.5 | 5 | 2.5 | 5 | 2.5 | 5 | 2.5 | 5 | V/ns |

Description : SR : Slew Rate
Q : Query Output (like in DQ, which stands for Data-in, Query-Output)
se : Single-ended Signals
For Ron = RZQ/7 setting

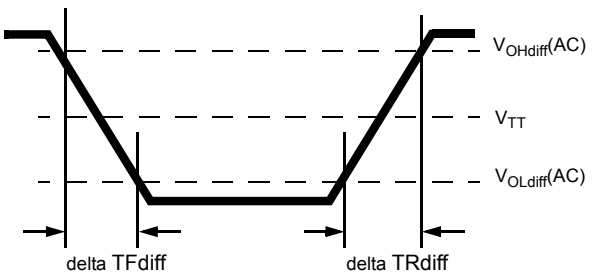


**Figure 6. Single-ended output slew rate definition**

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## 14.4 Differential Output Slew Rate

With the reference load for timing measurements, output slew rate for falling and rising edges is defined and measured between $V_{OLdiff}(AC)$ and $V_{OH-diff}(AC)$ for differential signals as shown in below.

**[ Table 12 ] Differential Output slew rate definition**

| Description | Measured | | Defined by |
|---|---|---|---|
| | From | To | |
| Differential output slew rate for rising edge | $V_{OLdiff}(AC)$ | $V_{OHdiff}(AC)$ | $\frac{V_{OHdiff}(AC)-V_{OLdiff}(AC)}{\text{Delta TRdiff}}$ |
| Differential output slew rate for falling edge | $V_{OHdiff}(AC)$ | $V_{OLdiff}(AC)$ | $\frac{V_{OHdiff}(AC)-V_{OLdiff}(AC)}{\text{Delta TFdiff}}$ |

**NOTE** : Output slew rate is verified by design and characterization, and may not be subject to production test.

**[ Table 13 ] Differential Output slew rate**

| Parameter | Symbol | DDR3-800 | | DDR3-1066 | | DDR3-1333 | | DDR3-1600 | | Units |
|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| Differential output slew rate | SRQdiff | 5 | 10 | 5 | 10 | 5 | 10 | 5 | 10 | V/ns |

Description : SR : Slew Rate
Q : Query Output (like in DQ, which stands for Data-in, Query-Output)
diff : Differential Signals
For Ron = RZQ/7 setting

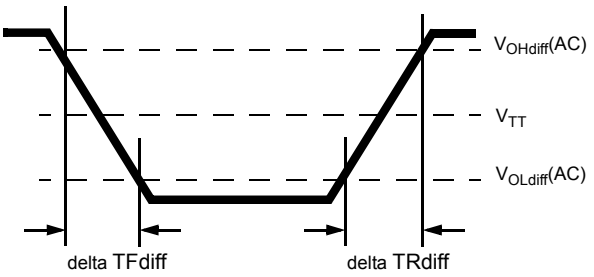


**Figure 7. Differential output slew rate definition**

# 15. DIMM IDD specification definition

| Symbol | Description |
|---|---|
| IDD0 | **Operating One Bank Active-Precharge Current**<br>**CKE:** High; **External clock:** On; **tCK, nRC, nRAS, CL:** Refer to Component Datasheet for detail pattern ; **BL**: 8[1]; **AL**: 0; **$\overline{CS}$**: High between ACT and PRE; **Command, Address, Bank Address Inputs:** partially toggling ; **Data IO:** FLOATING; **DM:**stable at 0; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... ; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern |
| IDD1 | **Operating One Bank Active-Read-Precharge Current**<br>**CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, CL:** Refer to Component Datasheet for detail pattern ; **BL**: 8[1]; **AL**: 0; **$\overline{CS}$**: High between ACT, RD and PRE; **Command, Address, Bank Address Inputs, Data IO:** partially toggling ; **DM:**stable at 0; **Bank Activity:** Cycling with one bank active at a time: 0,0,1,1,2,2,... ; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern |
| IDD2N | **Precharge Standby Current**<br>**CKE:** High; **External clock:** On; **tCK, CL:** Refer to Component Datasheet for detail pattern ; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$**: stable at 1; **Command, Address, Bank Address Inputs:** partially toggling ; **Data IO:** FLOATING; **DM:**stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern |
| IDD2P0 | **Precharge Power-Down Current Slow Exit**<br>**CKE:** Low; **External clock:** On; **tCK, CL:** Refer to Component Datasheet for detail pattern ; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** FLOATING; **DM:**stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Precharge Power Down Mode:** Slow Exit[3] |
| IDD2P1 | **Precharge Power-Down Current Fast Exit**<br>**CKE:** Low; **External clock:** On; **tCK, CL:** Refer to Component Datasheet for detail pattern ; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** FLOATING; **DM:**stable at 0; **Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Precharge Power Down Mode:** Fast Exit[3] |
| IDD2Q | **Precharge Quiet Standby Current**<br>**CKE:** High; **External clock:** On; **tCK, CL:** Refer to Component Datasheet for detail pattern ; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** FLOATING; **DM:**stable at 0;**Bank Activity:** all banks closed; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0 |
| IDD3N | **Active Standby Current**<br>**CKE:** High; **External clock:** On; **tCK, CL:** Refer to Component Datasheet for detail pattern ; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$**: stable at 1; **Command, Address, Bank Address Inputs:** partially toggling ; **Data IO:** FLOATING; **DM:**stable at 0;**Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern |
| IDD3P | **Active Power-Down Current**<br>**CKE:** Low; **External clock:** On; **tCK, CL:** Refer to Component Datasheet for detail pattern ; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$**: stable at 1; **Command, Address, Bank Address Inputs:** stable at 0; **Data IO:** FLOATING;**DM**:stable at 0; **Bank Activity:** all banks open; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0 |
| IDD4R | **Operating Burst Read Current**<br>**CKE:** High; **External clock:** On; **tCK, CL:** Refer to Component Datasheet for detail pattern ; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$**: High between RD; **Command, Address, Bank Address Inputs:** partially toggling ; **Data IO:** seamless read data burst with different data between one burst and the next one ; **DM:**stable at 0; **Bank Activity:** all banks open, **RD commands cycling through banks:** 0,0,1,1,2,2,... ; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern |
| IDD4W | **Operating Burst Write Current**<br>**CKE:** High; **External clock:** On; **tCK, CL:** Refer to Component Datasheet for detail pattern ; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$**: High between WR; **Command, Address, Bank Address Inputs:** partially toggling ; **Data IO:** seamless write data burst with different data between one burst and the next one ; **DM:** stable at 0; **Bank Activity:** all banks open, **WR commands cycling through banks:** 0,0,1,1,2,2,... ; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at HIGH; **Pattern Details:** Refer to Component Datasheet for detail pattern |
| IDD5B | **Burst Refresh Current**<br>**CKE:** High; **External clock:** On; **tCK, CL, nRFC:** Refer to Component Datasheet for detail pattern ; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$**: High between REF; **Command, Address, Bank Address Inputs:** partially toggling ; **Data IO:** FLOATING;**DM:**stable at 0; **Bank Activity:** REF command every nRFC ; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern |
| IDD6 | **Self Refresh Current: Normal Temperature Range**<br>**TCASE:** 0 - 85°C; **Auto Self-Refresh (ASR):** Disabled[4]; **Self-Refresh Temperature Range (SRT): N**ormal[5]; **CKE:** Low; **External clock:** Off; **CK and $\overline{CK}$:** LOW; **CL:** Refer to Component Datasheet for detail pattern ; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$**, **Command, Address, Bank Address, Data IO:** FLOATING;**DM:**stable at 0; **Bank Activity:** Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** FLOATING |
| IDD6ET | **Self-Refresh Current: Extended Temperature Range (optional)**[6]<br>**TCASE:** 0 - 95°C; **Auto Self-Refresh (ASR):** Disabled[4]; **Self-Refresh Temperature Range (SRT):** Extended[5]; CKE: Low; **External clock:** Off; **CK and $\overline{CK}$:** LOW; **CL:** Refer to Component Datasheet for detail pattern ; **BL:** 8[1]; **AL:** 0; **$\overline{CS}$**, Command, Address, Bank Address, **Data IO:** FLOATING;**DM:**stable at 0; **Bank Activity:** Extended Temperature Self-Refresh operation; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** FLOATING |
| IDD7 | **Operating Bank Interleave Read Current**<br>**CKE:** High; **External clock:** On; **tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL:** Refer to Component Datasheet for detail pattern ; **BL:** 8[1]; **AL:** CL-1; **$\overline{CS}$**: High between ACT and RDA; **Command, Address, Bank Address Inputs:** partially toggling ; **Data IO:** read data bursts with different data between one burst and the next one ; **DM:**stable at 0; **Bank Activity:** two times interleaved cycling through banks (0, 1, ...7) with different addressing ; **Output Buffer and RTT:** Enabled in Mode Registers[2]; **ODT Signal:** stable at 0; **Pattern Details:** Refer to Component Datasheet for detail pattern |
| IDD8 | **RESET Low Current**<br>**RESET :** Low; **External clock :** off; **CK and $\overline{CK}$** : LOW; **CKE** : FLOATING ; **$\overline{CS}$, Command, Address, Bank Address, Data IO** : FLOATING ; **ODT Signal :** FLOATING |

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**NOTE** :

1) Burst Length: BL8 fixed by MRS: set MR0 A[1,0]=00B
2) Output Buffer Enable: set MR1 A[12] = 0B; set MR1 A[5,1] = 01B; RTT_Nom enable: set MR1 A[9,6,2] = 011B; RTT_Wr enable: set MR2 A[10,9] = 10B
3) Precharge Power Down Mode: set MR0 A12=0B for Slow Exit or MR0 A12=1B for Fast Exit
4) Auto Self-Refresh (ASR): set MR2 A6 = 0B to disable or 1B to enable feature
5) Self-Refresh Temperature Range (SRT): set MR2 A7=0B for normal or 1B for extended temperature range
6) Refer to DRAM supplier data sheet and/or DIMM SPD to determine if optional features or requirements are supported by DDR3 SDRAM device
7) IDD current measure method and detail patterns are described on DDR3 component datasheet
8) VDD and VDDQ are merged on module PCB.
9) DIMM IDD SPEC is measured with Qoff condition
   (IDDQ values are not considered)

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# 16. IDD SPEC Table

### M393B2G70AH0 : 16GB(2Gx72) Module

| Symbol | CF8 (DDR3-1066@CL=7) | CH9 (DDR3-1333@CL=9) | Unit | NOTE |
|---|---|---|---|---|
| IDD0 | 2020 | 2240 | mA | 1 |
| IDD1 | 2200 | 2420 | mA | 1 |
| IDD2P0(slow exit) | 1110 | 1150 | mA | |
| IDD2P1(fast exit) | 1290 | 1330 | mA | |
| IDD2N | 1540 | 1760 | mA | |
| IDD2Q | 1520 | 1560 | mA | |
| IDD3P | 1470 | 1510 | mA | |
| IDD3N | 2070 | 2290 | mA | |
| IDD4R | 2560 | 2960 | mA | 1 |
| IDD4W | 2750 | 3150 | mA | 1 |
| IDD5B | 3780 | 4270 | mA | 1 |
| IDD6 | 1100 | 1140 | mA | |
| IDD7 | 3910 | 4670 | mA | 1 |
| IDD8 | 1100 | 1140 | mA | |

**NOTE** :
1. DIMM IDD SPEC is calculated with considering de-actived rank(IDLE) is IDD2N.

### M393B2G73AH0 : 16GB(2Gx72) Module

| Symbol | CF8 (DDR3-1066@CL=7) | CH9 (DDR3-1333@CL=9) | Unit | NOTE |
|---|---|---|---|---|
| IDD0 | 1795 | 2015 | mA | 1 |
| IDD1 | 1930 | 2150 | mA | 1 |
| IDD2P0(slow exit) | 1110 | 1150 | mA | |
| IDD2P1(fast exit) | 1290 | 1330 | mA | |
| IDD2N | 1540 | 1760 | mA | |
| IDD2Q | 1520 | 1560 | mA | |
| IDD3P | 1470 | 1510 | mA | |
| IDD3N | 2070 | 2290 | mA | |
| IDD4R | 2200 | 2510 | mA | 1 |
| IDD4W | 2300 | 2700 | mA | 1 |
| IDD5B | 2700 | 3010 | mA | 1 |
| IDD6 | 1100 | 1140 | mA | |
| IDD7 | 2830 | 3365 | mA | 1 |
| IDD8 | 1100 | 1140 | mA | |

**NOTE** :
1. DIMM IDD SPEC is calculated with considering de-actived rank(IDLE) is IDD2N.

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### M393B4G70AM0 : 32GB(4Gx72) Module

| Symbol | CF8 (DDR3-1066@CL=7) | CH9 (DDR3-1333@CL=9) | Unit | NOTE |
|---|---|---|---|---|
| IDD0 | 3456 | 3888 | mA | 1 |
| IDD1 | 3636 | 4068 | mA | 1 |
| IDD2P0(slow exit) | 2106 | 2178 | mA | |
| IDD2P1(fast exit) | 2466 | 2538 | mA | |
| IDD2N | 2952 | 3384 | mA | |
| IDD2Q | 2916 | 2988 | mA | |
| IDD3P | 2826 | 2898 | mA | |
| IDD3N | 4014 | 4446 | mA | |
| IDD4R | 3996 | 4608 | mA | 1 |
| IDD4W | 4194 | 4806 | mA | 1 |
| IDD5B | 5184 | 5886 | mA | 1 |
| IDD6 | 2088 | 2160 | mA | |
| IDD7 | 5346 | 6318 | mA | 1 |
| IDD8 | 2088 | 2160 | mA | |

**NOTE** :
1. DIMM IDD SPEC is calculated with considering de-actived rank(IDLE) is IDD2N.

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# 17. Input/Output Capacitance

| Parameter | Symbol | M393B2G70AH0 | | | | Units | NOTE |
|---|---|---|---|---|---|---|---|
| | | DDR3-1066 | | DDR3-1333 | | | |
| | | Min | Max | Min | Max | | |
| Input/output capacitance (DQ, DM, DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$) | CIO | - | TBD | - | TBD | pF | |
| Input capacitance (CK and $\overline{CK}$) | CCK | - | TBD | - | TBD | pF | |
| Input capacitance (All other input-only pins) | CI | - | TBD | - | TBD | - | |

| Parameter | Symbol | M393B2G73AH0 | | | | Units | NOTE |
|---|---|---|---|---|---|---|---|
| | | DDR3-1066 | | DDR3-1333 | | | |
| | | Min | Max | Min | Max | | |
| Input/output capacitance (DQ, DM, DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$) | CIO | - | TBD | - | TBD | pF | |
| Input capacitance (CK and $\overline{CK}$) | CCK | - | TBD | - | TBD | pF | |
| Input capacitance (All other input-only pins) | CI | - | TBD | - | TBD | - | |

| Parameter | Symbol | M393B4G70AM0 | | | | Units | NOTE |
|---|---|---|---|---|---|---|---|
| | | DDR3-1066 | | DDR3-1333 | | | |
| | | Min | Max | Min | Max | | |
| Input/output capacitance (DQ, DM, DQS, $\overline{DQS}$, TDQS, $\overline{TDQS}$) | CIO | - | TBD | - | TBD | pF | |
| Input capacitance (CK and $\overline{CK}$) | CCK | - | TBD | - | TBD | pF | |
| Input capacitance (All other input-only pins) | CI | - | TBD | - | TBD | - | |

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# 18. Electrical Characteristics and AC timing

(0 °C<$T_{CASE}$ ≤95 °C, $V_{DDQ}$ = 1.5V ± 0.075V; $V_{DD}$ = 1.5V ± 0.075V)

## 18.1 Refresh Parameters by Device Density

| Parameter | Symbol | | 1Gb | 2Gb | 4Gb | 8Gb | Units | NOTE |
|---|---|---|---|---|---|---|---|---|
| All Bank Refresh to active/refresh cmd time | tRFC | | 110 | 160 | 300 | 350 | ns | |
| Average periodic refresh interval | tREFI | 0 °C ≤ $T_{CASE}$ ≤ 85°C | 7.8 | 7.8 | 7.8 | 7.8 | µs | |
| | | 85 °C < $T_{CASE}$ ≤ 95°C | 3.9 | 3.9 | 3.9 | 3.9 | µs | 1 |

**NOTE** :

1. Users should refer to the DRAM supplier data sheet and/or the DIMM SPD to determine if DDR3 SDRAM devices support the following options or requirements referred to in this material.

## 18.2 Speed Bins and CL, tRCD, tRP, tRC and tRAS for Corresponding Bin

| Speed | DDR3-800 | DDR3-1066 | DDR3-1333 | DDR3-1600 | Units | NOTE |
|---|---|---|---|---|---|---|
| Bin (CL - tRCD - tRP) | 6-6-6 | 7-7-7 | 9-9-9 | 11-11-11 | | |
| Parameter | min | min | min | min | | |
| CL | 6 | 7 | 9 | 11 | tCK | |
| tRCD | 15 | 13.13 | 13.5 | 13.75 | ns | |
| tRP | 15 | 13.13 | 13.5 | 13.75 | ns | |
| tRAS | 37.5 | 37.5 | 36 | 35 | ns | |
| tRC | 52.5 | 50.63 | 49.5 | 48.75 | ns | |
| tRRD | 10 | 7.5 | 6.0 | 6.0 | ns | |
| tFAW | 40 | 37.5 | 30 | 30 | ns | |

## 18.3 Speed Bins and CL, tRCD, tRP, tRC and tRAS for corresponding Bin

DDR3 SDRAM Speed Bins include tCK, tRCD, tRP, tRAS and tRC for each corresponding bin.

**[ Table 14 ] DDR3-800 Speed Bins**

| Speed | | DDR3-800 | | Units | NOTE |
|---|---|---|---|---|---|
| CL-nRCD-nRP | | 6 - 6 - 6 | | | |
| Parameter | Symbol | min | max | | |
| Internal read command to first data | tAA | 15 | 20 | ns | |
| ACT to internal read or write delay time | tRCD | 15 | - | ns | |
| PRE command period | tRP | 15 | - | ns | |
| ACT to ACT or REF command period | tRC | 52.5 | - | ns | |
| ACT to PRE command period | tRAS | 37.5 | 9*tREFI | ns | |
| CL = 6 / CWL = 5 | tCK(AVG) | 2.5 | 3.3 | ns | 1,2,3 |
| Supported CL Settings | | 6 | | nCK | |
| Supported CWL Settings | | 5 | | nCK | |

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**[ Table 15 ] DDR3-1066 Speed Bins**

| Speed | | | DDR3-1066 | | Units | NOTE |
|---|---|---|---|---|---|---|
| CL-nRCD-nRP | | | 7 - 7 - 7 | | | |
| Parameter | | Symbol | min | max | | |
| Internal read command to first data | | tAA | 13.125 | 20 | ns | |
| ACT to internal read or write delay time | | tRCD | 13.125 | - | ns | |
| PRE command period | | tRP | 13.125 | - | ns | |
| ACT to ACT or REF command period | | tRC | 50.625 | - | ns | |
| ACT to PRE command period | | tRAS | 37.5 | 9*tREFI | ns | |
| CL = 6 | CWL = 5 | tCK(AVG) | 2.5 | 3.3 | ns | 1,2,3,5 |
| | CWL = 6 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| CL = 7 | CWL = 5 | tCK(AVG) | Reserved | | ns | 4 |
| | CWL = 6 | tCK(AVG) | 1.875 | <2.5 | ns | 1,2,3,4,8 |
| CL = 8 | CWL = 5 | tCK(AVG) | Reserved | | ns | 4 |
| | CWL = 6 | tCK(AVG) | 1.875 | <2.5 | ns | 1,2,3 |
| Supported CL Settings | | | 6,7,8 | | nCK | |
| Supported CWL Settings | | | 5,6 | | nCK | |

**[ Table 16 ] DDR3-1333 Speed Bins**

| Speed | | | DDR3-1333 | | Units | NOTE |
|---|---|---|---|---|---|---|
| CL-nRCD-nRP | | | 9 -9 - 9 | | | |
| Parameter | | Symbol | min | max | | |
| Internal read command to first data | | tAA | 13.5 (13.125)[8] | 20 | ns | |
| ACT to internal read or write delay time | | tRCD | 13.5 (13.125)[8] | - | ns | |
| PRE command period | | tRP | 13.5 (13.125)[8] | - | ns | |
| ACT to ACT or REF command period | | tRC | 49.5 (49.125)[8] | - | ns | |
| ACT to PRE command period | | tRAS | 36 | 9*tREFI | ns | |
| CL = 6 | CWL = 5 | tCK(AVG) | 2.5 | 3.3 | ns | 1,2,3,6 |
| | CWL = 6 | tCK(AVG) | Reserved | | ns | 1,2,3,4,6 |
| | CWL = 7 | tCK(AVG) | Reserved | | ns | 4 |
| CL = 7 | CWL = 5 | tCK(AVG) | Reserved | | ns | 4 |
| | CWL = 6 | tCK(AVG) | 1.875 | <2.5 | ns | 1,2,3,4,6 |
| | CWL = 7 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| CL = 8 | CWL = 5 | tCK(AVG) | Reserved | | ns | 4 |
| | CWL = 6 | tCK(AVG) | 1.875 | <2.5 | ns | 1,2,3,6 |
| | CWL = 7 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| CL = 9 | CWL = 5,6 | tCK(AVG) | Reserved | | ns | 4 |
| | CWL = 7 | tCK(AVG) | 1.5 | <1.875 | ns | 1,2,3,4,8 |
| CL = 10 | CWL = 5,6 | tCK(AVG) | Reserved | | ns | 4 |
| | CWL = 7 | tCK(AVG) | Reserved | | ns | 1,2,3 |
| Supported CL Settings | | | 6,7,8,9 | | nCK | |
| Supported CWL Settings | | | 5,6,7 | | nCK | |

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**[ Table 17 ] DDR3-1600 Speed Bins**

| Speed | | | DDR3-1600 | | Units | NOTE |
|---|---|---|---|---|---|---|
| CL-nRCD-nRP | | | 11-11-11 | | | |
| Parameter | | Symbol | min | max | | |
| Internal read command to first data | | tAA | 13.75 (13.125)[8] | 20 | ns | |
| ACT to internal read or write delay time | | tRCD | 13.75 (13.125)[8] | - | ns | |
| PRE command period | | tRP | 13.75 (13.125)[8] | - | ns | |
| ACT to ACT or REF command period | | tRC | 48.75 (48.125)[8] | - | ns | |
| ACT to PRE command period | | tRAS | 35 | 9*tREFI | ns | |
| CL = 6 | CWL = 5 | tCK(AVG) | 2.5 | 3.3 | ns | 1,2,3,7 |
| | CWL = 6 | tCK(AVG) | Reserved | | ns | 1,2,3,4,7 |
| | CWL = 7, 8 | tCK(AVG) | Reserved | | ns | 4 |
| CL = 7 | CWL = 5 | tCK(AVG) | Reserved | | ns | 4 |
| | CWL = 6 | tCK(AVG) | 1.875 | <2.5 | ns | 1,2,3,4,7 |
| | CWL = 7 | tCK(AVG) | Reserved | | ns | 1,2,3,4,7 |
| | CWL = 8 | tCK(AVG) | Reserved | | ns | 4 |
| CL = 8 | CWL = 5 | tCK(AVG) | Reserved | | ns | 4 |
| | CWL = 6 | tCK(AVG) | 1.875 | <2.5 | ns | 1,2,3,7 |
| | CWL = 7 | tCK(AVG) | Reserved | | ns | 1,2,3,4,7 |
| | CWL = 8 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| CL = 9 | CWL = 5,6 | tCK(AVG) | Reserved | | ns | 4 |
| | CWL = 7 | tCK(AVG) | 1.5 | <1.875 | ns | 1,2,3,4,7 |
| | CWL = 8 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| CL = 10 | CWL = 5,6 | tCK(AVG) | Reserved | | ns | 4 |
| | CWL = 7 | tCK(AVG) | 1.5 | <1.875 | ns | 1,2,3,7 |
| | CWL = 8 | tCK(AVG) | Reserved | | ns | 1,2,3,4 |
| CL = 11 | CWL = 5,6,7 | tCK(AVG) | Reserved | | ns | 4 |
| | CWL = 8 | tCK(AVG) | 1.25 | <1.5 | ns | 1,2,3,8 |
| Supported CL Settings | | | 6,7,8,9,10,11 | | nCK | |
| Supported CWL Settings | | | 5,6,7,8 | | nCK | |

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### 18.3.1 Speed Bin Table Notes

Absolute Specification ($T_{OPER}$; $V_{DDQ}$ = $V_{DD}$ = 1.5V +/- 0.075 V);

**NOTE** :

1. The CL setting and CWL setting result in tCK(AVG).MIN and tCK(AVG).MAX requirements. When making a selection of tCK(AVG), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(AVG).MIN limits: Since CAS Latency is not purely analog - data and strobe output are synchronized by the DLL - all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(AVG) value (2.5, 1.875, 1.5, or 1.25 ns) when calculating CL [nCK] = tAA [ns] / tCK(AVG) [ns], rounding up to the next "SupportedCL".
3. tCK(AVG).MAX limits: Calculate tCK(AVG) = tAA.MAX / CL SELECTED and round the resulting tCK(AVG) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875 ns or 1.25 ns). This result is tCK(AVG).MAX corresponding to CL SELECTED.
4. "Reserved" settings are not allowed. User must program a different value.
5. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
6. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
7. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table which are not subject to Production Tests but verified by Design/ Characterization.
8. For devices supporting optional downshift to CL=7 and CL=9, tAA/tRCD/tRP min must be 13.125 ns or lower. SPD settings must be programmed to match. For example, DDR3-1333(CL9) devices supporting downshift to DDR3-1066(CL7) should program 13.125 ns in SPD bytes for tAAmin (Byte 16), tRCDmin (Byte 18), and tRPmin (Byte 20). DDR3-1600(CL11) devices supporting downshift to DDR3-1333(CL9) or DDR3-1066(CL7) should program 13.125 ns in SPD bytes for tAAmin (Byte16), tRCDmin (Byte 18), and tRPmin (Byte 20). Once tRP (Byte 20) is programmed to 13.125ns, tRCmin (Byte 21,23) also should be programmed accordingly. For example, 49.125ns (tRASmin + tRPmin=36ns+13.125ns) for DDR3-1333(CL9) and 48.125ns (tRASmin+tRPmin=35ns+13.125ns) for DDR3-1600(CL11).

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# 19. Timing Parameters by Speed Grade

**[ Table 18 ] Timing Parameters by Speed Bin**

| Speed | | DDR3-800 | | DDR3-1066 | | DDR3-1333 | | DDR3-1600 | | Units | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | |
| **Clock Timing** | | | | | | | | | | | |
| Minimum Clock Cycle Time (DLL off mode) | tCK(DLL_OFF) | 8 | - | 8 | - | 8 | - | 8 | - | ns | 6 |
| Average Clock Period | tCK(avg) | See Speed Bins Table | | | | | | | | ps | |
| Clock Period | tCK(abs) | tCK(avg)min + tJIT(per)min | tCK(avg)max + tJIT(per)max | tCK(avg)min + tJIT(per)min | tCK(avg)max + tJIT(per)max | tCK(avg)min + tJIT(per)min | tCK(avg)max + tJIT(per)max | tCK(avg)min + tJIT(per)min | tCK(avg)max + tJIT(per)max | ps | |
| Average high pulse width | tCH(avg) | 0.47 | 0.53 | 0.47 | 0.53 | 0.47 | 0.53 | 0.47 | 0.53 | tCK(avg) | |
| Average low pulse width | tCL(avg) | 0.47 | 0.53 | 0.47 | 0.53 | 0.47 | 0.53 | 0.47 | 0.53 | tCK(avg) | |
| Clock Period Jitter | tJIT(per) | -100 | 100 | -90 | 90 | -80 | 80 | -70 | 70 | ps | |
| Clock Period Jitter during DLL locking period | tJIT(per, lck) | -90 | 90 | -80 | 80 | -70 | 70 | -60 | 60 | ps | |
| Cycle to Cycle Period Jitter | tJIT(cc) | 200 | | 180 | | 160 | | 140 | | ps | |
| Cycle to Cycle Period Jitter during DLL locking period | tJIT(cc, lck) | 180 | | 160 | | 140 | | 120 | | ps | |
| Cumulative error across 2 cycles | tERR(2per) | - 147 | 147 | - 132 | 132 | - 118 | 118 | -103 | 103 | ps | |
| Cumulative error across 3 cycles | tERR(3per) | - 175 | 175 | - 157 | 157 | - 140 | 140 | -122 | 122 | ps | |
| Cumulative error across 4 cycles | tERR(4per) | - 194 | 194 | - 175 | 175 | - 155 | 155 | -136 | 136 | ps | |
| Cumulative error across 5 cycles | tERR(5per) | - 209 | 209 | - 188 | 188 | - 168 | 168 | -147 | 147 | ps | |
| Cumulative error across 6 cycles | tERR(6per) | - 222 | 222 | - 200 | 200 | - 177 | 177 | -155 | 155 | ps | |
| Cumulative error across 7 cycles | tERR(7per) | - 232 | 232 | - 209 | 209 | - 186 | 186 | -163 | 163 | ps | |
| Cumulative error across 8 cycles | tERR(8per) | - 241 | 241 | - 217 | 217 | - 193 | 193 | -169 | 169 | ps | |
| Cumulative error across 9 cycles | tERR(9per) | - 249 | 249 | - 224 | 224 | - 200 | 200 | -175 | 175 | ps | |
| Cumulative error across 10 cycles | tERR(10per) | - 257 | 257 | - 231 | 231 | - 205 | 205 | -180 | 180 | ps | |
| Cumulative error across 11 cycles | tERR(11per) | - 263 | 263 | - 237 | 237 | - 210 | 210 | -184 | 184 | ps | |
| Cumulative error across 12 cycles | tERR(12per) | - 269 | 269 | - 242 | 242 | - 215 | 215 | -188 | 188 | ps | |
| Cumulative error across n = 13, 14 ... 49, 50 cycles | tERR(nper) | tERR(nper)min = (1 + 0.68ln(n))*tJIT(per)min<br>tERR(nper)max = (1 + 0.68ln(n))*tJIT(per)max | | | | | | | | ps | 24 |
| Absolute clock HIGH pulse width | tCH(abs) | 0.43 | - | 0.43 | - | 0.43 | - | 0.43 | - | tCK(avg) | 25 |
| Absolute clock Low pulse width | tCL(abs) | 0.43 | - | 0.43 | - | 0.43 | - | 0.43 | - | tCK(avg) | 26 |
| **Data Timing** | | | | | | | | | | | |
| DQS,$\overline{DQS}$ to DQ skew, per group, per access | tDQSQ | - | 200 | - | 150 | - | 125 | - | 100 | ps | 13 |
| DQ output hold time from DQS, $\overline{DQS}$ | tQH | 0.38 | - | 0.38 | - | 0.38 | - | 0.38 | - | tCK(avg) | 13, g |
| DQ low-impedance time from CK, $\overline{CK}$ | tLZ(DQ) | -800 | 400 | -600 | 300 | -500 | 250 | -450 | 225 | ps | 13,14, f |
| DQ high-impedance time from CK, $\overline{CK}$ | tHZ(DQ) | - | 400 | - | 300 | - | 250 | - | 225 | ps | 13,14, f |
| Data setup time to DQS, $\overline{DQS}$ referenced to $V_{IH}(AC)V_{IL}(AC)$ levels | tDS(base) AC175 | 75 | - | 25 | - | - | - | - | | ps | d, 17 |
| | tDS(base) AC150 | 125 | - | 75 | - | 30 | - | 10 | | ps | d, 17 |
| Data hold time to DQS, $\overline{DQS}$ referenced to $V_{IH}(AC)V_{IL}(AC)$ levels | tDH(base) DC100 | 150 | - | 100 | - | 65 | - | 45 | | ps | d, 17 |
| DQ and DM Input pulse width for each input | tDIPW | 600 | - | 490 | - | 400 | - | 360 | | ps | 28 |
| **Data Strobe Timing** | | | | | | | | | | | |
| DQS, $\overline{DQS}$ differential READ Preamble | tRPRE | 0.9 | NOTE 19 | 0.9 | NOTE 19 | 0.9 | NOTE 19 | 0.9 | NOTE 19 | tCK | 13, 19, g |
| DQS, $\overline{DQS}$ differential READ Postamble | tRPST | 0.3 | NOTE 11 | 0.3 | NOTE 11 | 0.3 | NOTE 11 | 0.3 | NOTE 11 | tCK | 11, 13, b |
| DQS, $\overline{DQS}$ differential output high time | tQSH | 0.38 | - | 0.38 | - | 0.4 | - | 0.4 | - | tCK(avg) | 13, g |
| DQS, $\overline{DQS}$ differential output low time | tQSL | 0.38 | - | 0.38 | - | 0.4 | - | 0.4 | - | tCK(avg) | 13, g |
| DQS, $\overline{DQS}$ differential WRITE Preamble | tWPRE | 0.9 | - | 0.9 | - | 0.9 | - | 0.9 | - | tCK | |
| DQS, $\overline{DQS}$ differential WRITE Postamble | tWPST | 0.3 | - | 0.3 | - | 0.3 | - | 0.3 | - | tCK | |
| DQS, $\overline{DQS}$ rising edge output access time from rising CK, $\overline{CK}$ | tDQSCK | -400 | 400 | -300 | 300 | -255 | 255 | -225 | 225 | ps | 13,f |
| DQS, $\overline{DQS}$ low-impedance time (Referenced from RL-1) | tLZ(DQS) | -800 | 400 | -600 | 300 | -500 | 250 | -450 | 225 | ps | 13,14,f |
| DQS, $\overline{DQS}$ high-impedance time (Referenced from RL+BL/2) | tHZ(DQS) | - | 400 | - | 300 | - | 250 | - | 225 | ps | 12,13,14 |
| DQS, $\overline{DQS}$ differential input low pulse width | tDQSL | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | tCK | 29, 31 |
| DQS, $\overline{DQS}$ differential input high pulse width | tDQSH | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | tCK | 30, 31 |
| DQS, $\overline{DQS}$ rising edge to CK, $\overline{CK}$ rising edge | tDQSS | -0.25 | 0.25 | -0.25 | 0.25 | -0.25 | 0.25 | -0.27 | 0.27 | tCK(avg) | c |
| DQS,$\overline{DQS}$ falling edge setup time to CK, $\overline{CK}$ rising edge | tDSS | 0.2 | - | 0.2 | - | 0.2 | - | 0.18 | - | tCK(avg) | c, 32 |
| DQS,$\overline{DQS}$ falling edge hold time to CK, $\overline{CK}$ rising edge | tDSH | 0.2 | - | 0.2 | - | 0.2 | - | 0.18 | - | tCK(avg) | c, 32 |

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**[ Table 18 ] Timing Parameters by Speed Bin (Cont.)**

| Speed | | DDR3-800 | | DDR3-1066 | | DDR3-1333 | | DDR3-1600 | | Units | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | |
| **Command and Address Timing** | | | | | | | | | | | |
| DLL locking time | tDLLK | 512 | - | 512 | - | 512 | - | 512 | - | nCK | |
| internal READ Command to PRECHARGE Command delay | tRTP | max (4nCK,7.5ns ) | - | max (4nCK,7.5ns) | - | max (4nCK,7.5ns) | - | max (4nCK,7.5ns) | - | | e |
| Delay from start of internal write transaction to internal read command | tWTR | max (4nCK,7.5ns ) | - | max (4nCK,7.5ns) | - | max (4nCK,7.5ns) | - | max (4nCK,7.5ns) | - | | e,18 |
| WRITE recovery time | tWR | 15 | - | 15 | - | 15 | - | 15 | - | ns | e |
| Mode Register Set command cycle time | tMRD | 4 | - | 4 | - | 4 | - | 4 | - | nCK | |
| Mode Register Set command update delay | tMOD | max (12nCK,15n s) | - | max (12nCK,15ns ) | - | max (12nCK,15ns ) | - | max (12nCK,15ns) | - | | |
| CAS# to CAS# command delay | tCCD | 4 | - | 4 | - | 4 | - | 4 | - | nCK | |
| Auto precharge write recovery + precharge time | tDAL(min) | WR + roundup (tRP / tCK(AVG)) | | | | | | | | nCK | |
| Multi-Purpose Register Recovery Time | tMPRR | 1 | - | 1 | - | 1 | - | 1 | - | nCK | 22 |
| ACTIVE to PRECHARGE command period | tRAS | See “Speed Bins and CL, tRCD, tRP, tRC and tRAS for corresponding Bin” on page 42 | | | | | | | | ns | e |
| ACTIVE to ACTIVE command period for 1KB page size | tRRD | max (4nCK,10ns) | - | max (4nCK,7.5ns) | - | max (4nCK,6ns) | - | max (4nCK,6ns) | - | | e |
| ACTIVE to ACTIVE command period for 2KB page size | tRRD | max (4nCK,10ns) | - | max (4nCK,10ns) | - | max (4nCK,7.5ns) | - | max (4nCK,7.5ns) | - | | e |
| Four activate window for 1KB page size | tFAW | 40 | - | 37.5 | - | 30 | - | 30 | - | ns | e |
| Four activate window for 2KB page size | tFAW | 50 | - | 50 | - | 45 | - | 40 | - | ns | e |
| Command and Address setup time to CK, $\overline{CK}$ referenced to $V_{IH}$(AC) / $V_{IL}$(AC) levels | tIS(base) AC175 | 200 | - | 125 | - | 65 | - | 45 | - | ps | b,16 |
| | tIS(base) AC150 | 200 + 150 | - | 125 + 150 | - | 65+125 | - | 45+125 | - | ps | b,16,27 |
| Command and Address hold time from CK, $\overline{CK}$ referenced to $V_{IH}$(AC) / $V_{IL}$(AC) levels | tIH(base) DC100 | 275 | - | 200 | - | 140 | - | 120 | - | ps | b,16 |
| Control & Address Input pulse width for each input | tIPW | 900 | - | 780 | - | 620 | - | 560 | - | ps | 28 |
| **Calibration Timing** | | | | | | | | | | | |
| Power-up and RESET calibration time | tZQinitI | 512 | - | 512 | - | 512 | - | 512 | - | nCK | |
| Normal operation Full calibration time | tZQoper | 256 | - | 256 | - | 256 | - | 256 | - | nCK | |
| Normal operation short calibration time | tZQCS | 64 | - | 64 | - | 64 | - | 64 | - | nCK | 23 |
| **Reset Timing** | | | | | | | | | | | |
| Exit Reset from CKE HIGH to a valid command | tXPR | max(5nCK, tRFC + 10ns) | - | max(5nCK, tRFC + 10ns) | - | max(5nCK, tRFC + 10ns) | - | max(5nCK, tRFC + 10ns) | - | | |
| **Self Refresh Timing** | | | | | | | | | | | |
| Exit Self Refresh to commands not requiring a locked DLL | tXS | max(5nCK,t RFC + 10ns) | - | max(5nCK,tR FC + 10ns) | - | max(5nCK,tR FC + 10ns) | - | max(5nCK,tR FC + 10ns) | - | | |
| Exit Self Refresh to commands requiring a locked DLL | tXSDLL | tDLLK(min) | - | tDLLK(min) | - | tDLLK(min) | - | tDLLK(min) | - | nCK | |
| Minimum CKE low width for Self refresh entry to exit timing | tCKESR | tCKE(min) + 1tCK | - | tCKE(min) + 1tCK | - | tCKE(min) + 1tCK | - | tCKE(min) + 1tCK | - | | |
| Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE) | tCKSRE | max(5nCK, 10ns) | - | max(5nCK, 10ns) | - | max(5nCK, 10ns) | - | max(5nCK, 10ns) | - | | |
| Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit | tCKSRX | max(5nCK, 10ns) | - | max(5nCK, 10ns) | - | max(5nCK, 10ns) | - | max(5nCK, 10ns) | - | | |

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**[ Table 18 ] Timing Parameters by Speed Bin (Cont.)**

| Speed | | DDR3-800 | | DDR3-1066 | | DDR3-1333 | | DDR3-1600 | | Units | NOTE |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Parameter | Symbol | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | |
| **Power Down Timing** | | | | | | | | | | | |
| Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL | tXP | max (3nCK, 7.5ns) | - | max (3nCK, 7.5ns) | - | max (3nCK,6ns) | - | max (3nCK,6ns) | - | | |
| Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL | tXPDLL | max (10nCK, 24ns) | - | max (10nCK, 24ns) | - | max (10nCK, 24ns) | - | max (10nCK, 24ns) | - | | 2 |
| CKE minimum pulse width | tCKE | max (3nCK, 7.5ns) | - | max (3nCK, 5.625ns) | - | max (3nCK, 5.625ns) | - | max (3nCK,5ns) | - | | |
| Command pass disable delay | tCPDED | 1 | - | 1 | - | 1 | - | 1 | - | nCK | |
| Power Down Entry to Exit Timing | tPD | tCKE(min) | 9*tREFI | tCKE(min) | 9*tREFI | tCKE(min) | 9*tREFI | tCKE(min) | 9*tREFI | tCK | 15 |
| Timing of ACT command to Power Down entry | tACTPDEN | 1 | - | 1 | - | 1 | - | 1 | - | nCK | 20 |
| Timing of PRE command to Power Down entry | tPRPDEN | 1 | - | 1 | - | 1 | - | 1 | - | nCK | 20 |
| Timing of RD/RDA command to Power Down entry | tRDPDEN | RL + 4 +1 | - | RL + 4 +1 | - | RL + 4 +1 | - | RL + 4 +1 | - | | |
| Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF) | tWRPDEN | WL + 4 +(tWR/ tCK(avg)) | - | WL + 4 +(tWR/ tCK(avg)) | - | WL + 4 +(tWR/ tCK(avg)) | - | WL + 4 +(tWR/ tCK(avg)) | - | nCK | 9 |
| Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF) | tWRAPDEN | WL + 4 +WR +1 | - | WL + 4 +WR +1 | - | WL + 4 +WR +1 | - | WL + 4 +WR +1 | - | nCK | 10 |
| Timing of WR command to Power Down entry (BC4MRS) | tWRPDEN | WL + 2 +(tWR/ tCK(avg)) | - | WL + 2 +(tWR/ tCK(avg)) | - | WL + 2 +(tWR/ tCK(avg)) | - | WL + 2 +(tWR/ tCK(avg)) | - | nCK | 9 |
| Timing of WRA command to Power Down entry (BC4MRS) | tWRAPDEN | WL +2 +WR +1 | - | WL +2 +WR +1 | - | WL +2 +WR +1 | - | WL +2 +WR +1 | - | nCK | 10 |
| Timing of REF command to Power Down entry | tREFPDEN | 1 | - | 1 | - | 1 | - | 1 | - | | 20,21 |
| Timing of MRS command to Power Down entry | tMRSPDEN | tMOD(min) | - | tMOD(min) | - | tMOD(min) | - | tMOD(min) | - | | |
| **ODT Timing** | | | | | | | | | | | |
| ODT high time without write command or with write command and BC4 | ODTH4 | 4 | - | 4 | - | 4 | - | 4 | - | nCK | |
| ODT high time with Write command and BL8 | ODTH8 | 6 | - | 6 | - | 6 | - | 6 | - | nCK | |
| Asynchronous RTT turn-on delay (Power-Down with DLL frozen) | tAONPD | 2 | 8.5 | 2 | 8.5 | 2 | 8.5 | 2 | 8.5 | ns | |
| Asynchronous RTT turn-off delay (Power-Down with DLL frozen) | tAOFPD | 2 | 8.5 | 2 | 8.5 | 2 | 8.5 | 2 | 8.5 | ns | |
| RTT turn-on | tAON | -400 | 400 | -300 | 300 | -250 | 250 | -225 | 225 | ps | 7,f |
| RTT_NOM and RTT_WR turn-off time from ODTLoff reference | tAOF | 0.3 | 0.7 | 0.3 | 0.7 | 0.3 | 0.7 | 0.3 | 0.7 | tCK(avg) | 8,f |
| RTT dynamic change skew | tADC | 0.3 | 0.7 | 0.3 | 0.7 | 0.3 | 0.7 | 0.3 | 0.7 | tCK(avg) | f |
| **Write Leveling Timing** | | | | | | | | | | | |
| First DQS pulse rising edge after tDQSS margining mode is programmed | tWLMRD | 40 | - | 40 | - | 40 | - | 40 | - | tCK | 3 |
| DQS/DQS delay after tDQS margining mode is programmed | tWLDQSEN | 25 | - | 25 | - | 25 | - | 25 | - | tCK | 3 |
| Write leveling setup time from rising CK, $\overline{CK}$ crossing to rising DQS, $\overline{DQS}$ crossing | tWLS | 325 | - | 245 | - | 195 | - | 165 | - | ps | |
| Write leveling hold time from rising DQS, $\overline{DQS}$ crossing to rising CK, $\overline{CK}$ crossing | tWLH | 325 | - | 245 | - | 195 | - | 165 | - | ps | |
| Write leveling output delay | tWLO | 0 | 9 | 0 | 9 | 0 | 9 | 0 | 7.5 | ns | |
| Write leveling output error | tWLOE | 0 | 2 | 0 | 2 | 0 | 2 | 0 | 2 | ns | |

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## 19.1 Jitter Notes

**Specific Note a** Unit 'tCK(avg)' represents the actual tCK(avg) of the input clock under operation. Unit 'nCK' represents one clock cycle of the input clock, counting the actual clock edges.ex) tMRD = 4 [nCK] means; if one Mode Register Set command is registered at Tm, another Mode Register Set command may be registered at Tm+4, even if (Tm+4 - Tm) is 4 x tCK(avg) + tERR(4per),min.

**Specific Note b** These parameters are measured from a command/address signal (CKE, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, ODT, BA0, A0, A1, etc.) transition edge to its respective clock signal (CK/$\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as the setup and hold are relative to the clock signal crossing that latches the command/address. That is, these parameters should be met whether clock jitter is present or not.

**Specific Note c** These parameters are measured from a data strobe signal (DQS, $\overline{DQS}$) crossing to its respective clock signal (CK, $\overline{CK}$) crossing. The spec values are not affected by the amount of clock jitter applied (i.e. tJIT(per), tJIT(cc), etc.), as these are relative to the clock signal crossing. That is, these parameters should be met whether clock jitter is present or not.

**Specific Note d** These parameters are measured from a data signal (DM, DQ0, DQ1, etc.) transition edge to its respective data strobe signal (DQS, $\overline{DQS}$) crossing.

**Specific Note e** For these parameters, the DDR3 SDRAM device supports tnPARAM [nCK] = RU{ tPARAM [ns] / tCK(avg) [ns] }, which is in clock cycles, assuming all input clock jitter specifications are satisfied. For example, the device will support tnRP = RU{tRP / tCK(avg)}, which is in clock cycles, if all input clock jitter specifications are met. This means: For DDR3-800 6-6-6, of which tRP = 15ns, the device will support tnRP = RU{tRP / tCK(avg)} = 6, as long as the input clock jitter specifications are met, i.e. Precharge command at Tm and Active command at Tm+6 is valid even if (Tm+6 - Tm) is less than 15ns due to input clock jitter.

**Specific Note f** When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(mper),act of the input clock, where 2 <= m <= 12. (output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR3-800 SDRAM has tERR(mper),act,min = - 172 ps and tERR(mper),act,max = + 193 ps, then tDQSCK,min(derated) = tDQSCK,min - tERR(mper),act,max = - 400 ps - 193 ps = - 593 ps and tDQSCK,max(derated) = tDQSCK,max - tERR(mper),act,min = 400 ps + 172 ps = + 572 ps. Similarly, tLZ(DQ) for DDR3-800 derates to tLZ(DQ),min(derated) = - 800 ps - 193 ps = - 993 ps and tLZ(DQ),max(derated) = 400 ps + 172 ps = + 572 ps. (Caution on the min/max usage!)
Note that tERR(mper),act,min is the minimum measured value of tERR(nper) where 2 <= n <= 12, and tERR(mper),act,max is the maximum measured value of tERR(nper) where 2 <= n <= 12.

**Specific Note g** When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per),act of the input clock. (output deratings are relative to the SDRAM input clock.) For example, if the measured jitter into a DDR3-800 SDRAM has tCK(avg),act = 2500 ps, tJIT(per),act,min = - 72 ps and tJIT(per),act,max = + 93 ps, then tRPRE,min(derated) = tRPRE,min + tJIT(per),act,min = 0.9 x tCK(avg),act + tJIT(per),act,min = 0.9 x 2500 ps - 72 ps = + 2178 ps. Similarly, tQH,min(derated) = tQH,min + tJIT(per),act,min = 0.38 x tCK(avg),act + tJIT(per),act,min = 0.38 x 2500 ps - 72 ps = + 878 ps. (Caution on the min/max usage!)

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## 19.2 Timing Parameter Notes

1. Actual value dependant upon measurement level definitions which are TBD.
2. Commands requiring a locked DLL are: READ (and RAP) and synchronous ODT commands.
3. The max values are system dependent.
4. WR as programmed in mode register
5. Value must be rounded-up to next higher integer value
6. There is no maximum cycle time limit besides the need to satisfy the refresh interval, tREFI.
7. For definition of RTT turn-on time tAON see "Device Operation & Timing Diagram Datasheet"
8. For definition of RTT turn-off time tAOF see "Device Operation & Timing Diagram Datasheet".
9. tWR is defined in ns, for calculation of tWRPDEN it is necessary to round up tWR / tCK to the next integer.
10. WR in clock cycles as programmed in MR0
11. The maximum read postamble is bound by tDQSCK(min) plus tQSH(min) on the left side and tHZ(DQS)max on the right side. See "Device Operation & Timing Diagram Datasheet.
12. Output timing deratings are relative to the SDRAM input clock. When the device is operated with input clock jitter, this parameter needs to be derated by TBD
13. Value is only valid for RON34
14. Single ended signal parameter. Refer to chapter 8 and chapter 9 for definition and measurement method.
15. tREFI depends on $T_{OPER}$
16. tIS(base) and tIH(base) values are for 1V/ns CMD/ADD single-ended slew rate and 2V/ns CK, $\overline{CK}$ differential slew rate, Note for DQ and DM signals, $V_{REF}(DC) = V_{REF}DQ(DC)$. For input only pins except $\overline{RESET}$, $V_{REF}(DC)=V_{REF}CA(DC)$.
    See "Address/Command Setup, Hold and Derating" on component datasheet.
17. tDS(base) and tDH(base) values are for 1V/ns DQ single-ended slew rate and 2V/ns DQS, $\overline{DQS}$ differential slew rate. Note for DQ and DM signals, $V_{REF}(DC)= V_{REF}DQ(DC)$. For input only pins except $\overline{RESET}$, $V_{REF}(DC)=V_{REF}CA(DC)$.
    See "Data Setup, Hold and Slew Rate Derating" on component datasheet.
18. Start of internal write transaction is defined as follows ;
    For BL8 (fixed by MRS and on-the-fly) : Rising clock edge 4 clock cycles after WL.
    For BC4 (on-the-fly) : Rising clock edge 4 clock cycles after WL
    For BC4 (fixed by MRS) : Rising clock edge 2 clock cycles after WL
19. The maximum read preamble is bound by tLZDQS(min) on the left side and tDQSCK(max) on the right side. See "Device Operation & Timing Diagram Datasheet"
20. CKE is allowed to be registered low while operations such as row activation, precharge, autoprecharge or refresh are in progress, but power-down IDD spec will not be applied until finishing those operations.
21. Although CKE is allowed to be registered LOW after a REFRESH command once tREFPDEN(min) is satisfied, there are cases where additional time such as tXPDLL(min) is also required. See "Device Operation & Timing Diagram Datasheet".
22. Defined between end of MPR read burst and MRS which reloads MPR or disables MPR function.
23. One ZQCS command can effectively correct a minimum of 0.5 % (ZQCorrection) of RON and RTT impedance error within 64 nCK for all speed bins assuming the maximum sensitivities specified in the 'Output Driver Voltage and Temperature Sensitivity' and 'ODT Voltage and Temperature Sensitivity' tables. The appropriate interval between ZQCS commands can be determined from these tables and other application specific parameters.
    One method for calculating the interval between ZQCS commands, given the temperature (Tdriftrate) and voltage (Vdriftrate) drift rates that the SDRAM is subject to in the application, is illustrated. The interval could be defined by the following formula:

$$\frac{\text{ZQCorrection}}{(\text{TSens} \times \text{Tdriftrate}) + (\text{VSens} \times \text{Vdriftrate})}$$

where TSens = max(dRTTdT, dRONdTM) and VSens = max(dRTTdV, dRONdVM) define the SDRAM temperature and voltage sensitivities.

For example, if TSens = 1.5% /°C, VSens = 0.15% / mV, Tdriftrate = 1°C / sec and Vdriftrate = 15 mV / sec, then the interval between ZQCS commands is calculated as:

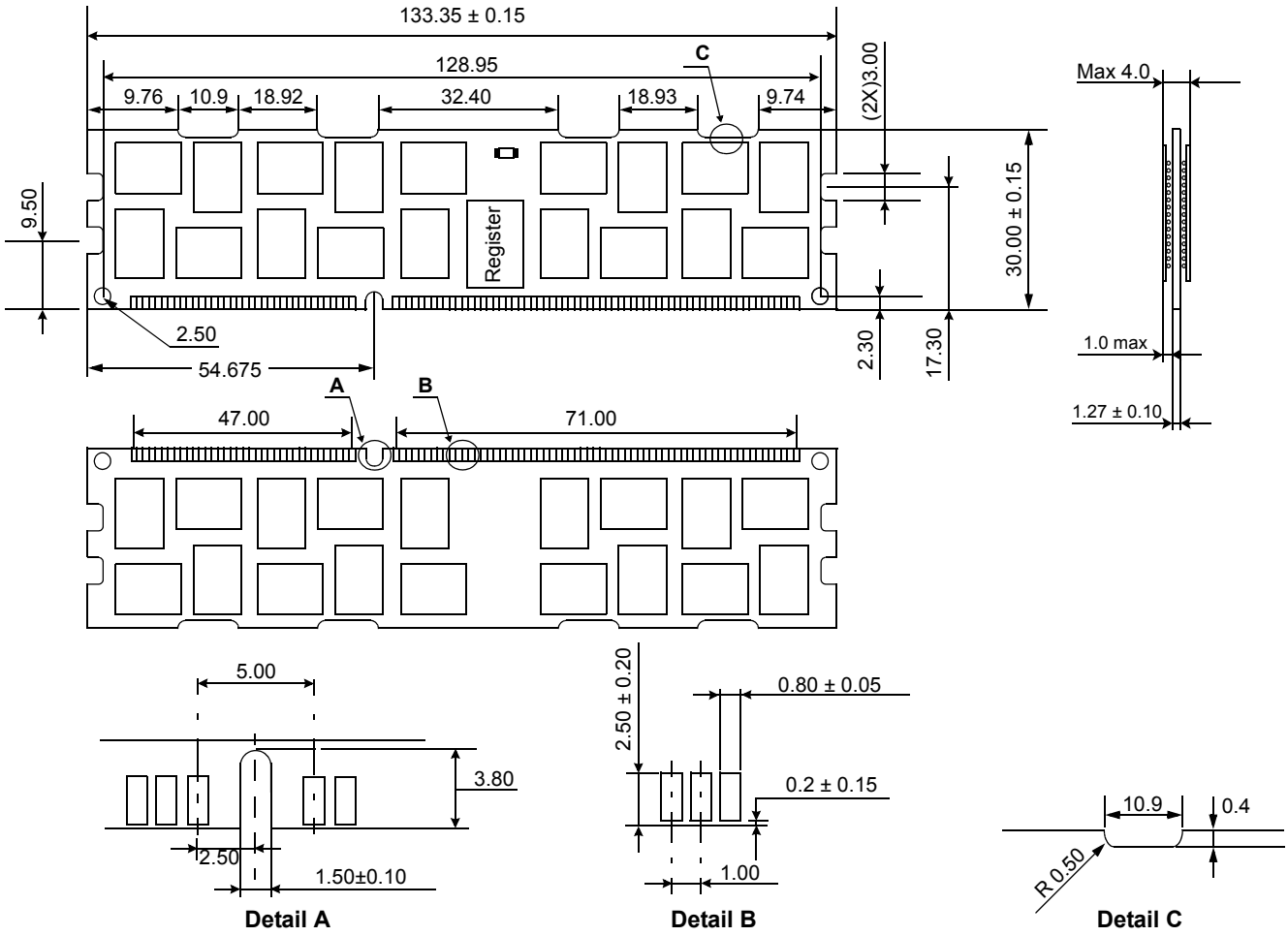
$$\frac{0.5}{(1.5 \times 1) + (0.15 \times 15)} = 0.133 \approx 128\text{ms}$$

24. n = from 13 cycles to 50 cycles. This row defines 38 parameters.
25. tCH(abs) is the absolute instantaneous clock high pulse width, as measured from one rising edge to the following falling edge.
26. tCL(abs) is the absolute instantaneous clock low pulse width, as measured from one falling edge to the following rising edge.
27. The tIS(base) AC150 specifications are adjusted from the tIS(base) specification by adding an additional 100 ps of derating to accommodate for the lower alternate threshold of 150 mV and another 25 ps to account for the earlier reference point [(175 mv - 150 mV) / 1 V/ns].
28. Pulse width of a input signal is defined as the width between the first crossing of $V_{REF}(DC)$ and the consecutive crossing of $V_{REF}(DC)$
29. tDQSL describes the instantaneous differential input low pulse width on DQS-$\overline{DQS}$, as measured from one falling edge to the next consecutive rising edge.
30. tDQSH describes the instantaneous differential input high pulse width on DQS-$\overline{DQS}$, as measured from one rising edge to the next consecutive falling edge.
31. tDQSH, act + tDQSL, act = 1 tCK, act ; with tXYZ, act being the actual measured value of the respective timing parameter in the application.
32. tDSH, act + tDSS, act = 1 tCK, act ; with tXYZ, act being the actual measured value of the respective timing parameter in the application.

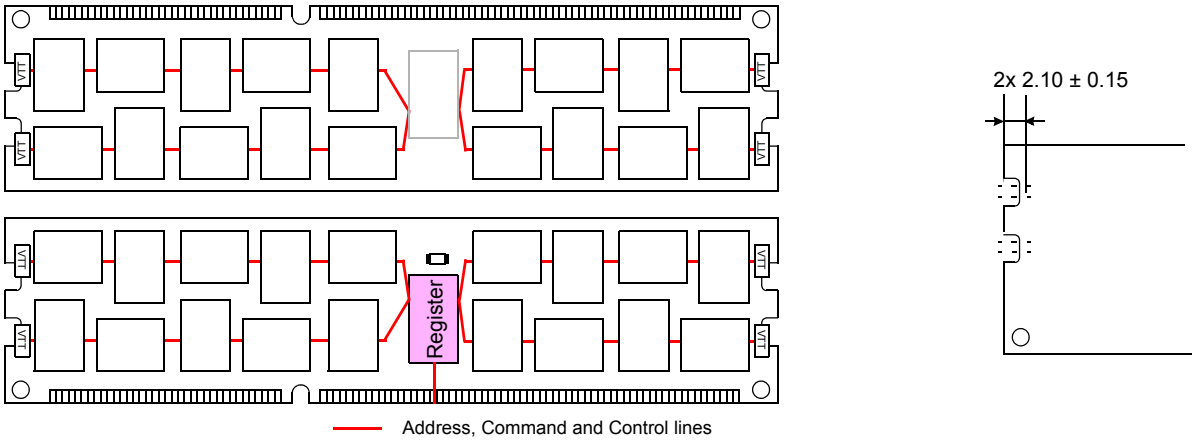
# 20. Physical Dimensions

## 20.1 1Gbx4 based 2Gx72 Module (2 Ranks) - M393B2G70AH0

Units : Millimeters




### 20.1.1 x72 DIMM, populated as two physical ranks of x4 DDR3 SDRAMs

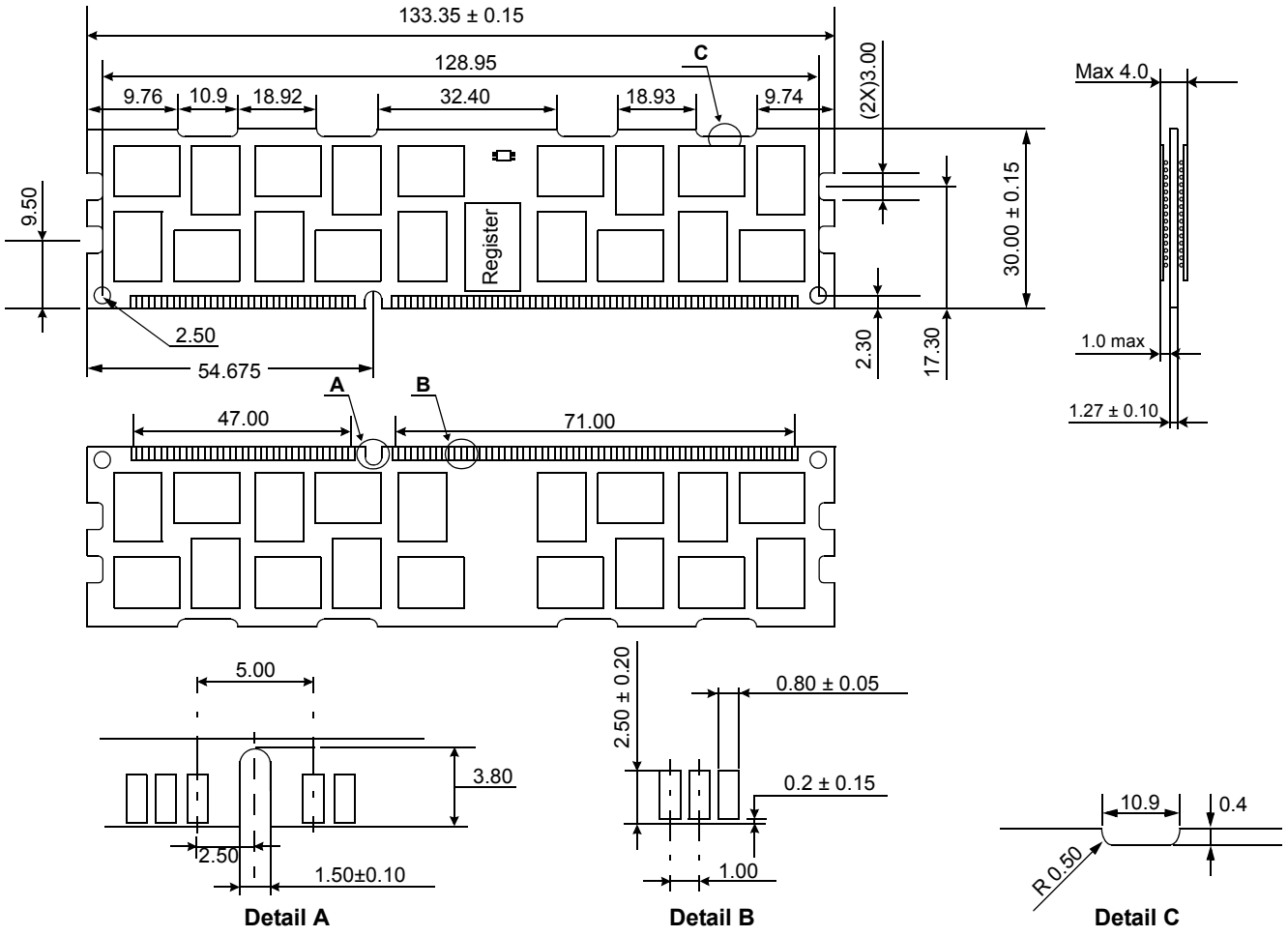



The used device is 1G x4 DDR3 SDRAM, FBGA.
DDR3 SDRAM Part NO : K4B4G0446A-HC**

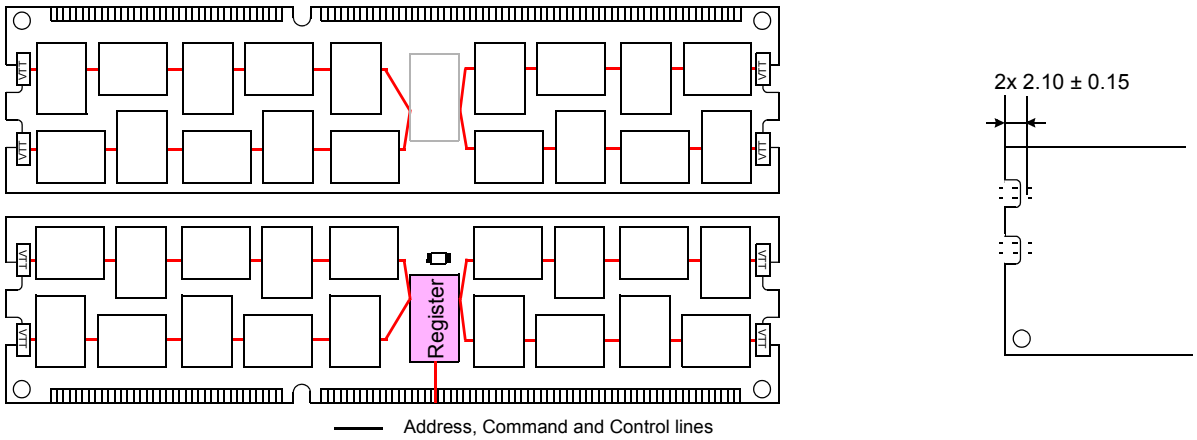
* **NOTE** : Tolerances on all dimensions ±0.15 unless otherwise specified.

## 20.2 512Mbx8 based 2Gx72 Module (4 Ranks) - M393B2G73AH0

Units : Millimeters




### 20.2.1 x72 DIMM, populated as four physical ranks of x8 DDR3 SDRAMs




The used device is 512M x8 DDR3 SDRAM, FBGA.
DDR3 SDRAM Part NO : K4B4G0846A-HC**

* **NOTE** : Tolerances on all dimensions ±0.15 unless otherwise specified.

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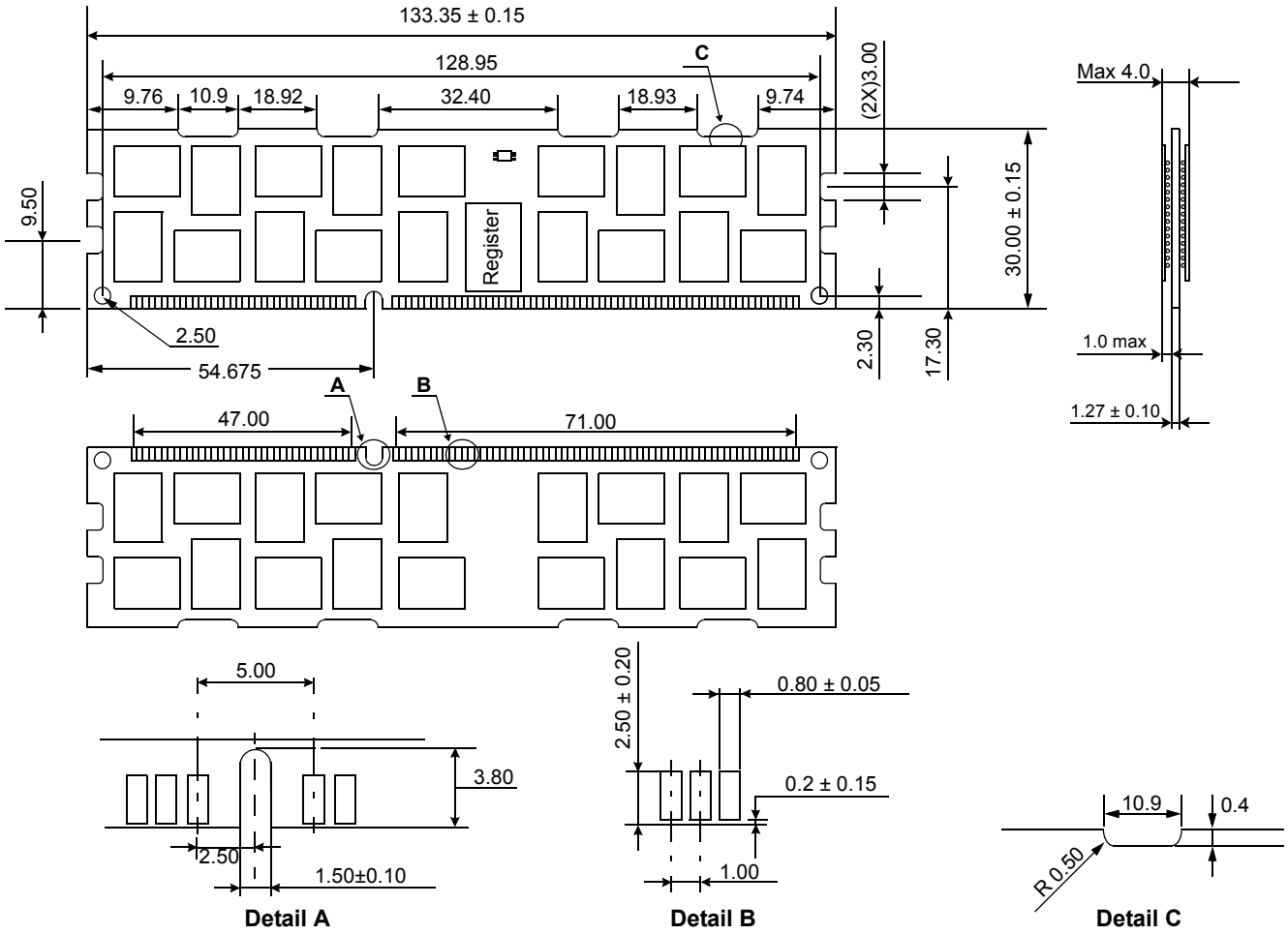
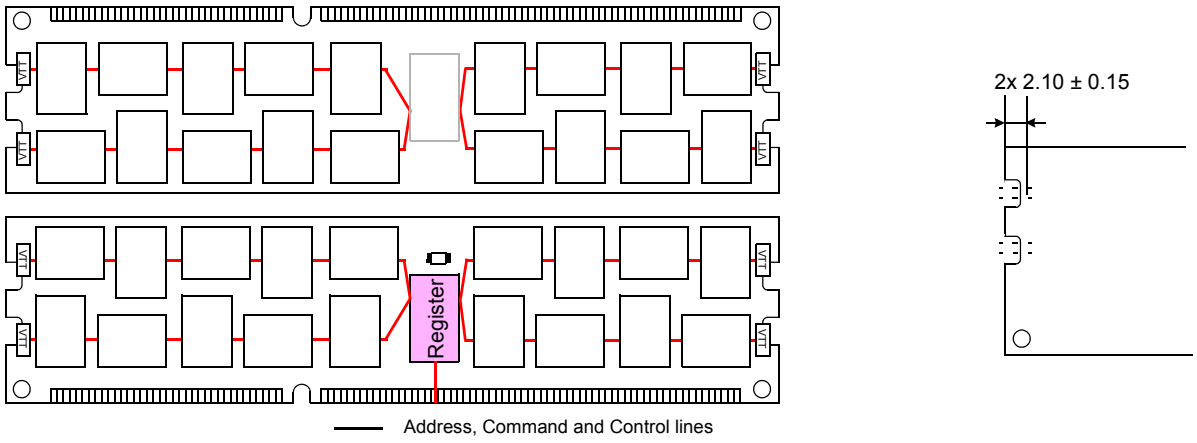
datasheet

## 20.3 2Gbx4(DDP) based 4Gx72 Module (4 Ranks) - M393B4G70AM0

Units : Millimeters




### 20.3.1 x72 DIMM, populated as four physical ranks of x4 DDR3 SDRAMs




The used device is 2G x4(DDP) DDR3 SDRAM, FBGA.
DDR3 SDRAM Part NO : K4B8G0446A-MC**

* **NOTE** : Tolerances on all dimensions ±0.15 unless otherwise specified.

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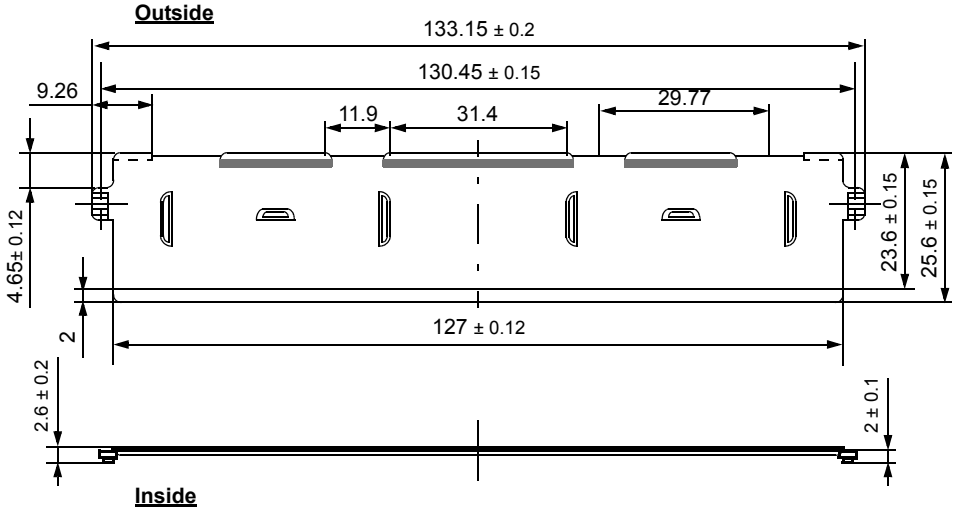
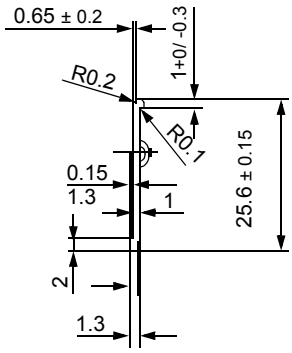
datasheet

## 20.3.2 Heat Spreader Design Guide

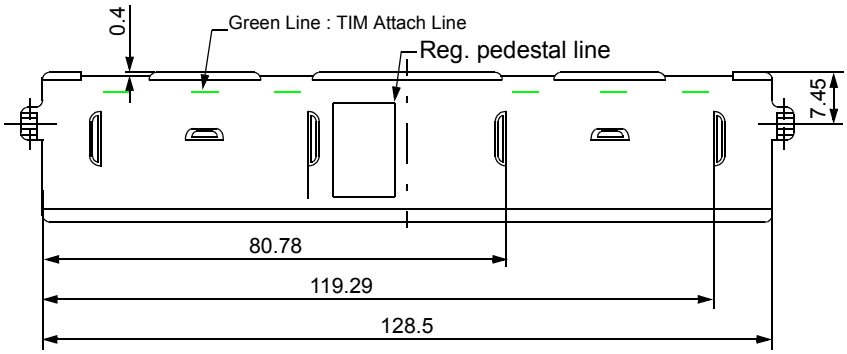
### 1. FRONT PART

**Outside**



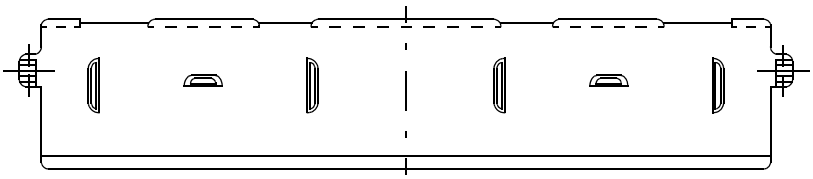




**Inside**

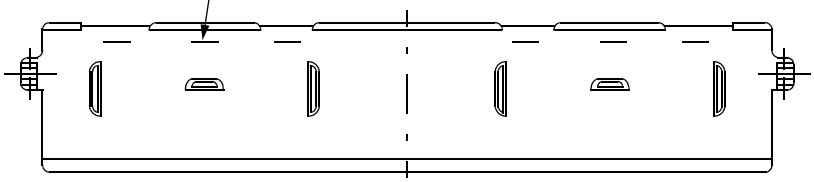



### 2. BACK PART

**Outside**



**Inside**



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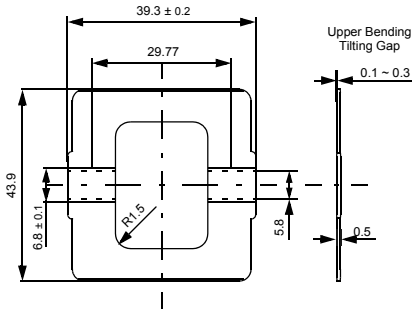
datasheet

### 3. CLIP PART




### 4. DDR3 RDIMM ASS'Y View

**Reference thickness total (Maximum) : 7.55 (With Clip thickness)**